英飛凌 CoolSiC™ 實現高效率電源供應系統

09.01.2021 **Max Hsu**

Agenda

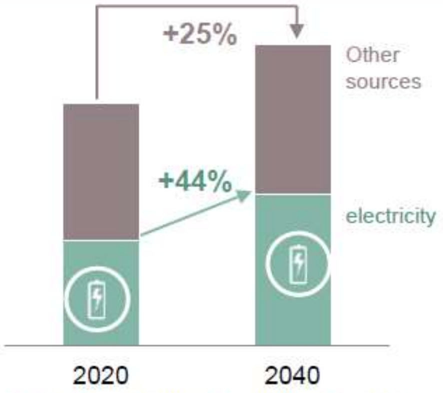
1. 電源供應市場需求變革
2. 第三代寬能隙半導體 (Wide Band Gap) 發展趨勢
3. CoolSiC™ & CoolMOS™ 特性分析與應用策略
4. 英飛淩 CoolSiC™ 產品應用優勢與方案介紹

1

電源供應市場需求變革

The global energy system faces a dual challenge: the need for more energy and less carbon

Primary energy demand[1]



Limit global warming at 1.5°C[2]

Global net human-caused **emissions of CO_2** need to **fall by about 45%** from 2010 levels by 2030

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1) Source: BP 2019 Energy Outlook | 2) Summary for Policymakers of IPCC Special Report on Global Warming of 1.5°C approved by governments

Global trends are driving demand for new power semiconductor solutions

Clean energy

Renewable energy sources like wind and sun are the vital part of new global energy mix

Energy efficiency

Reduction of energy consumed is needed, enabling systems that make the way we live and work greener

Electric mobility

Electrification of mobility is inevitable – in both, private and public transport segment

Silicon Carbide (SiC) could be an answer to some of these challenges and less carbon

New requirements & challenges

More **energy** from **clean resources**

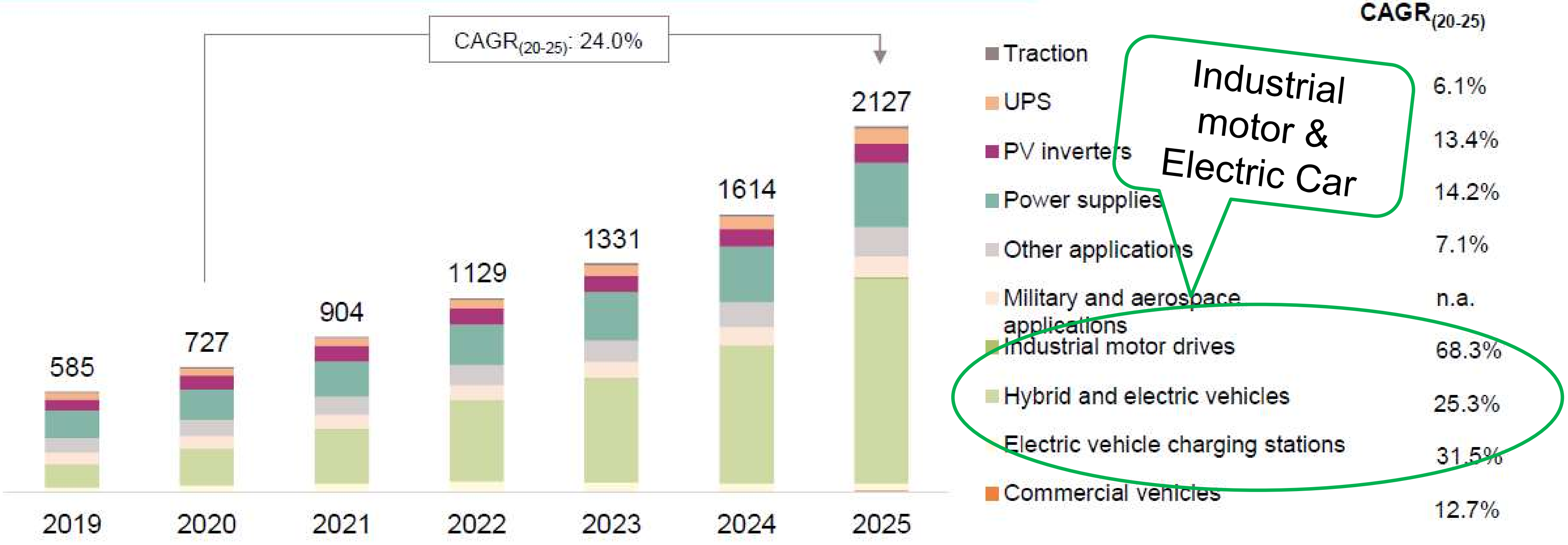
High-performance systems with **lower energy consumption**

Technical advantages of SiC lead to strong benefits for the system

- Increased performance
- Reduced system size
- Higher power density
- Lower system cost

As a result, more and more applications will start the adoption of SiC solutions and less carbon

SiC Power market development [m EUR]

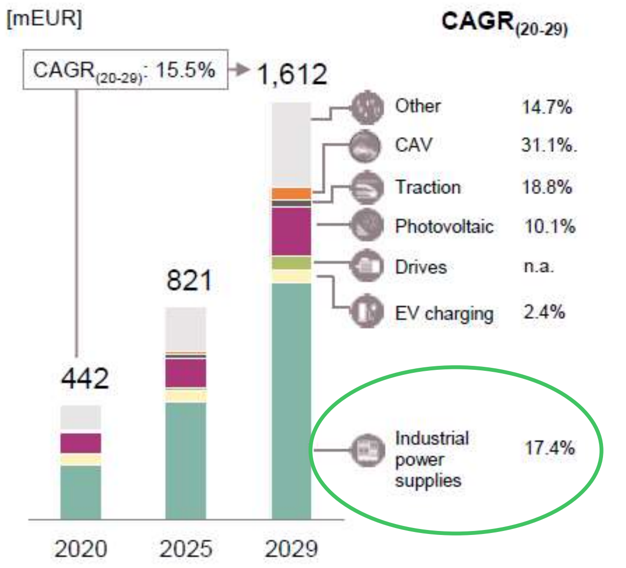


Industrial motor & Electric Car

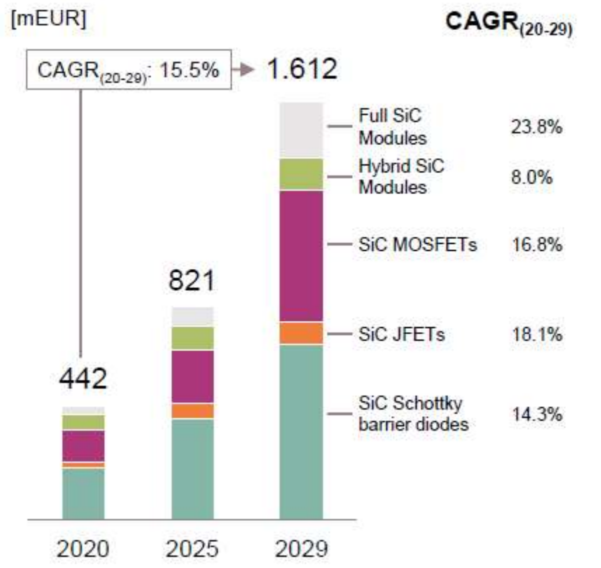
Original data from Omdia in USD, calculation of EUR with exchange rate of 1USD = 0,8933 EUR according to Omdia report below.
Sources: Based on or includes research from Omdia, SiC and GaN Power Semiconductor Market Report 2020 – June 2020, Mid case.
Results are not an endorsement of Infineon Technologies AG. Any reliance on these results is at the third party's own risk.

According to Omdia Industrial Power Supplies, Photovoltaic and Drives are the focus applications for SiC in the industrial landscape

SiC power semiconductors **by application**
excl. EV, Military & aerospace by **Omdia**



SiC power semiconductors **by product type**
excl. EV, Military & Aerospace by **Omdia**



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SiC will add significant value to a broad variety of systems across many applications

Photovoltaic
- reduction of system cost
- reduction of system size

EV charging
- faster charging cycles

IPS / UPS
- higher efficiency
- reduced total cost of ownership

tipping point reached

eMobility
- higher reach per charge
- more compact main inverter

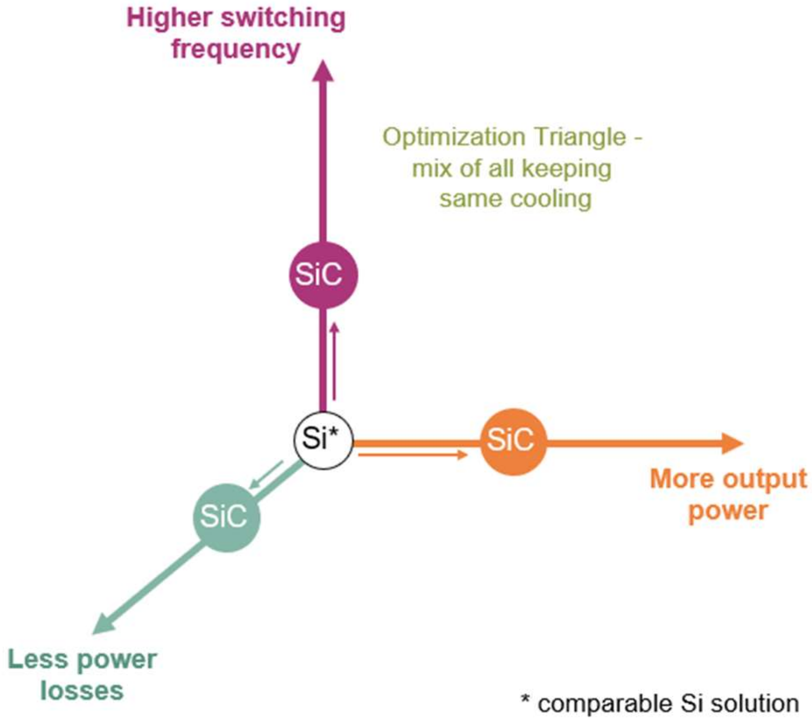
Traction
- lower system cost
- higher seat capacity

Drives
- reduced system size
- reduced total cost of ownership

future tipping points

2 第三代寬能隙半導體 (Wide Band Gap) 發展趨勢需求變革

Customers have the freedom to chose the optimum for their system when moving from Si to CoolSiC™ MOSFET

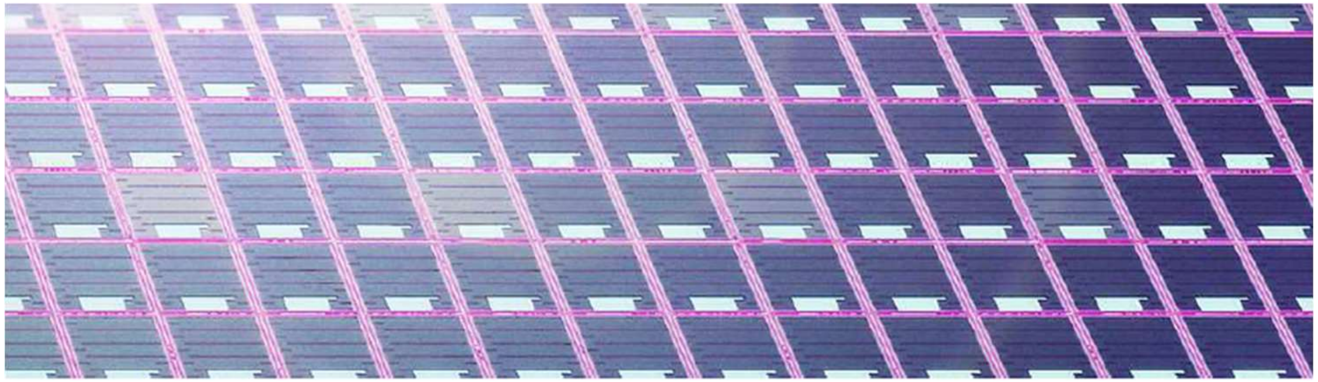


* comparable Si solution

Chose the optimum for your system:

- › Increase switching frequency with the same output power and total losses (keeping same cooling conditions)
  - ⇨ Reduce passive components
- › Get more output power with the same switching frequency and total losses (keeping same cooling conditions)
  - ⇨ Higher performance
- › Reduce the losses with the same switching frequency and same output power
  - ⇨ Better lifetime (keeping same cooling conditions)
  - ⇨ Saving on cooling (with the same lifetime)

Depending on application requirements Si, CoolSiC™ have specific value propositions



Silicon IGBT / MOSFET

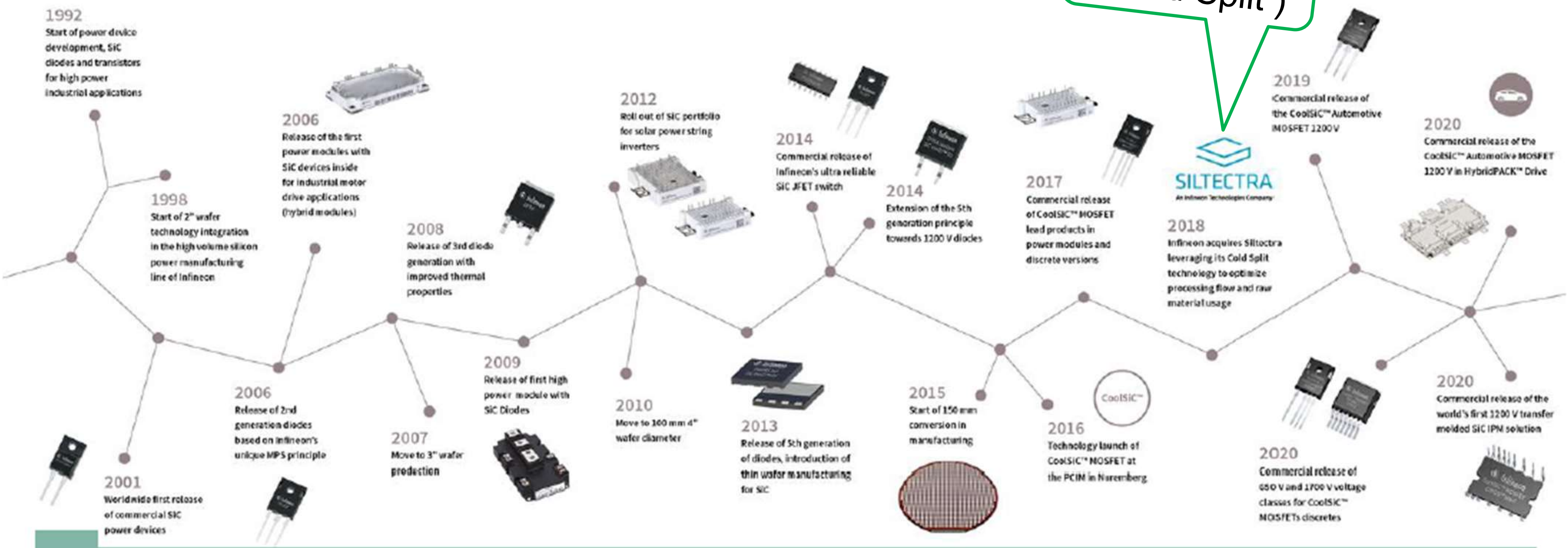
- Provides high flexibility as applicable across all power ranges
- Well known technology with decades of track record
- Lower device cost
- Broad range of chips and modules available

CoolSiC™ MOSFET

- Enables new levels of power density and performance
- Highest thermal conductivity
- Simpler topologies possible
- Smaller device footprint

Infineon has 20 years of field experience with SiC

冷切割技術
(Cold Split)



1992
Start of power device development, SiC diodes and transistors for high power industrial applications

1998
Start of 2" wafer technology integration in the high volume silicon power manufacturing line of Infineon

2001
Worldwide first release of commercial SiC power devices

2006
Release of 2nd generation diodes based on Infineon's unique MPS principle

2006
Release of the first power modules with SiC devices inside for industrial motor drive applications (hybrid modules)

2007
Move to 3" wafer production

2008
Release of 3rd diode generation with improved thermal properties

2009
Release of first high power module with SiC Diodes

2010
Move to 100 mm 4" wafer diameter

2012
Roll out of SiC portfolio for solar power string inverters

2013
Release of 5th generation of diodes, introduction of thin wafer manufacturing for SiC

2014
Commercial release of Infineon's ultra reliable SiC JFET switch

2014
Extension of the 5th generation principle towards 1200 V diodes

2015
Start of 150 mm conversion in manufacturing

2016
Technology launch of CoolSiC™ MOSFET at the PCIM in Nuremberg

2017
Commercial release of CoolSiC™ MOSFET lead products in power modules and discrete versions

2018
Infineon acquires Siltectra leveraging its Cold Split technology to optimize processing flow and raw material usage

2019
Commercial release of the CoolSiC™ Automotive MOSFET 1200 V

2020
Commercial release of the CoolSiC™ Automotive MOSFET 1200 V in HybridPACK™ Drive

2020
Commercial release of 650 V and 1700 V voltage classes for CoolSiC™ MOSFETs discretes

2020
Commercial release of the world's first 1200 V transfer molded SiC IPM solution

Numerous customers rely on Infineon, due to around 20 years of field experience

3 CoolSiC™ & CoolMOS™ 特性分析與應用策略

Why CoolSiC™?

SiC

Product and technology leadership	Infineon is a pioneer in Trench SiC MOSFET and CoolSiC™ is a comprehensive technology providing uncompromised performance
Unmatched quality and reliability	While our CoolSiC™ MOSFET comes with a superior gate oxide reliability, our production and qualification processes have been optimized >20 years enabling our superiority in chip and packaging
Secured manufacturing & supply	Infineon relies on a unique in-house capacity in both, front- and backend, a secured wafer supply and highly innovative manufacturing technologies (e.g. Cold Split)
Broad and best-in-class product portfolio	Our portfolio is optimized for the specific application requirements and ranges from SiC Diodes, through Discrete SiC MOSFETS to Hybrid and Full SiC Modules – complemented by Driver ICs

Silicon carbide chips offer advantages for power electronics

HIGHER VOLTAGE OPERATION

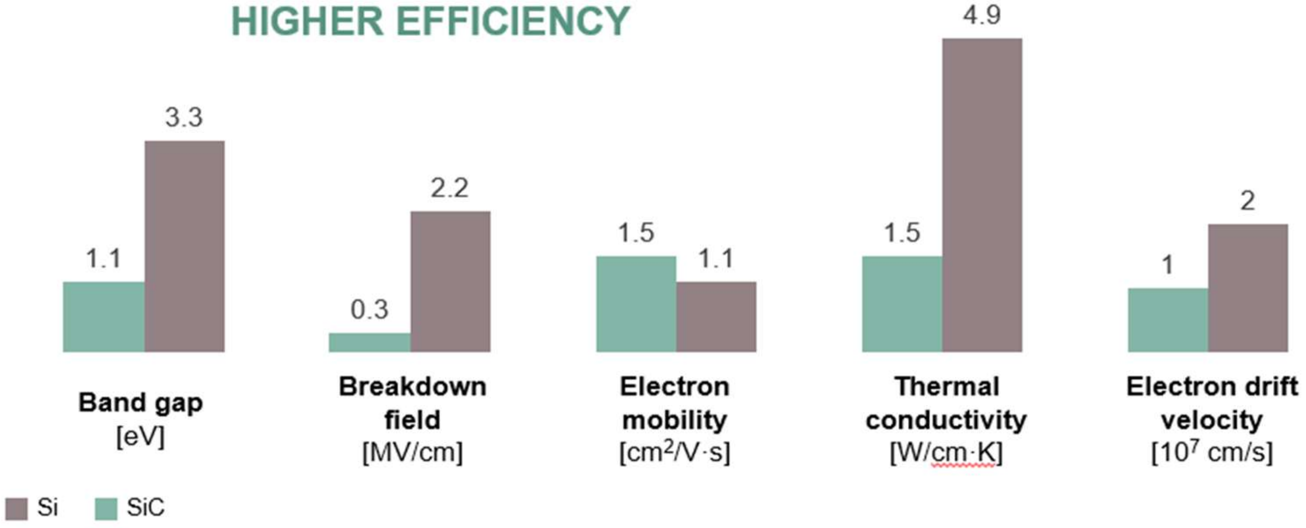
EXTENDED POWER DENSITY

HIGHER FREQUENCY SWITCHING

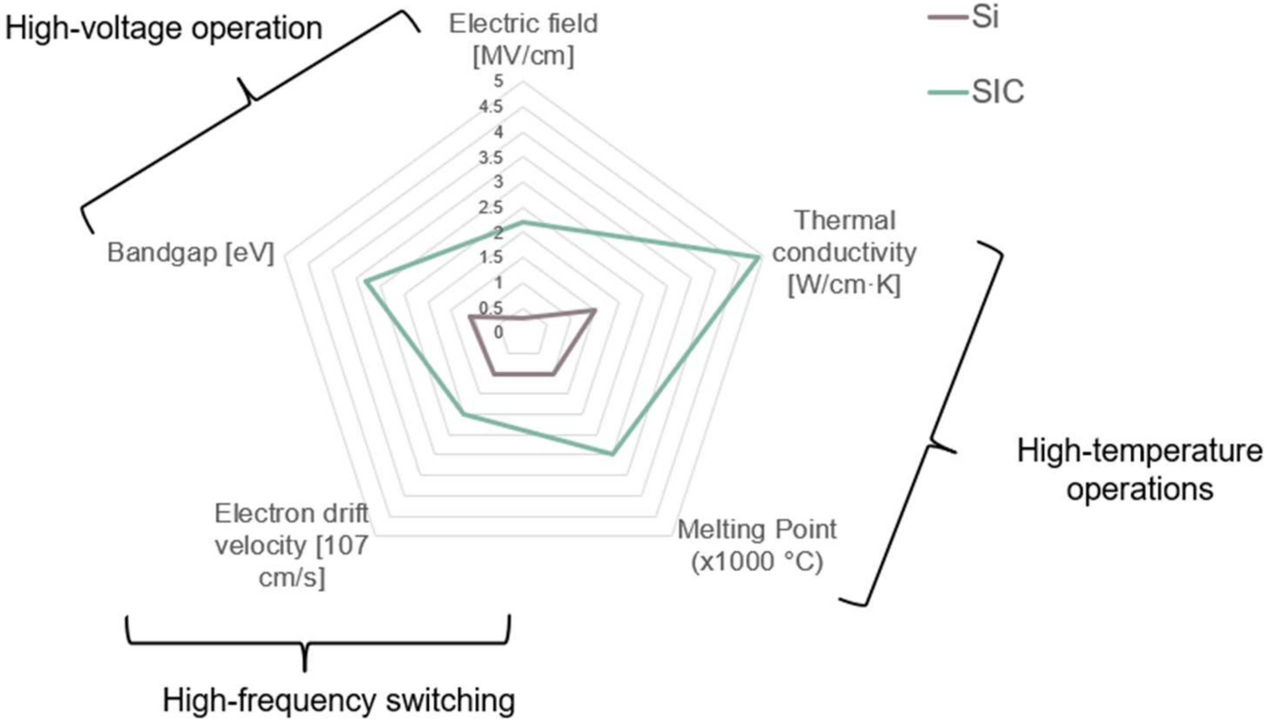
THINNER ACTIVE LAYERS

IMPROVED HEAT DISSIPATION

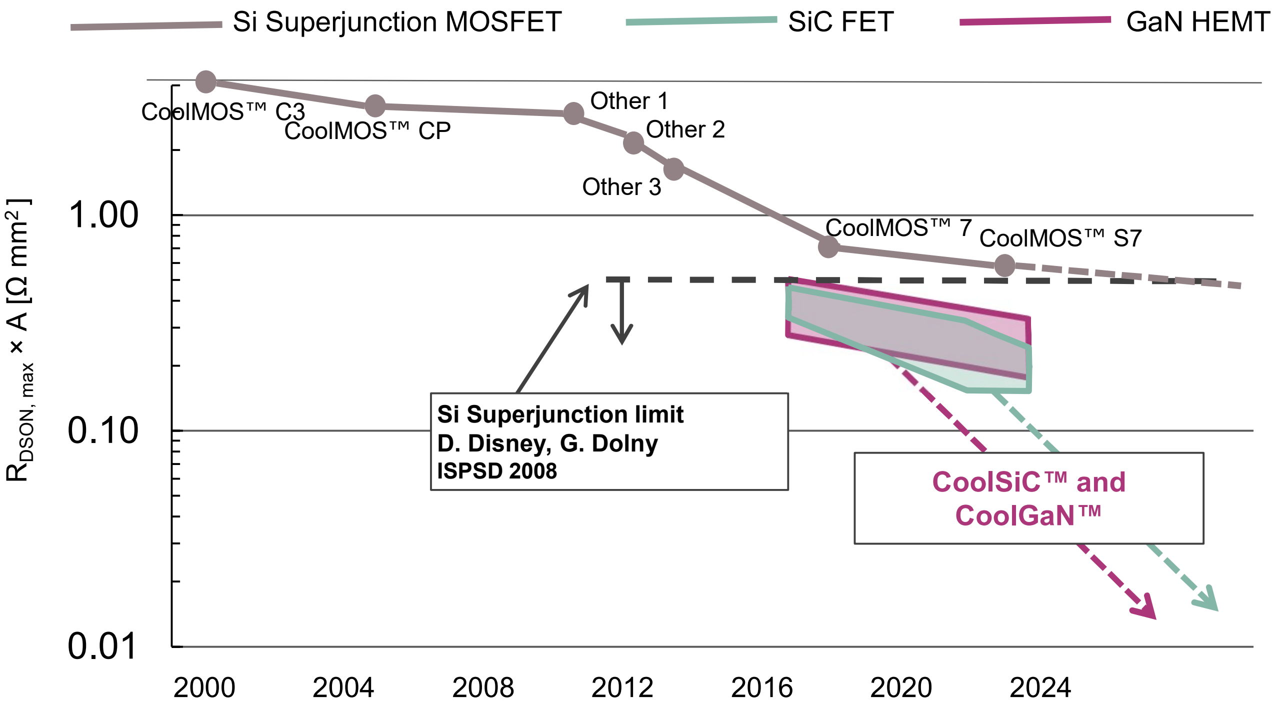
HIGHER EFFICIENCY



Application benefits leveraging SiC physical characteristics



R_{on} x A “roadmap” of HV semiconductor devices

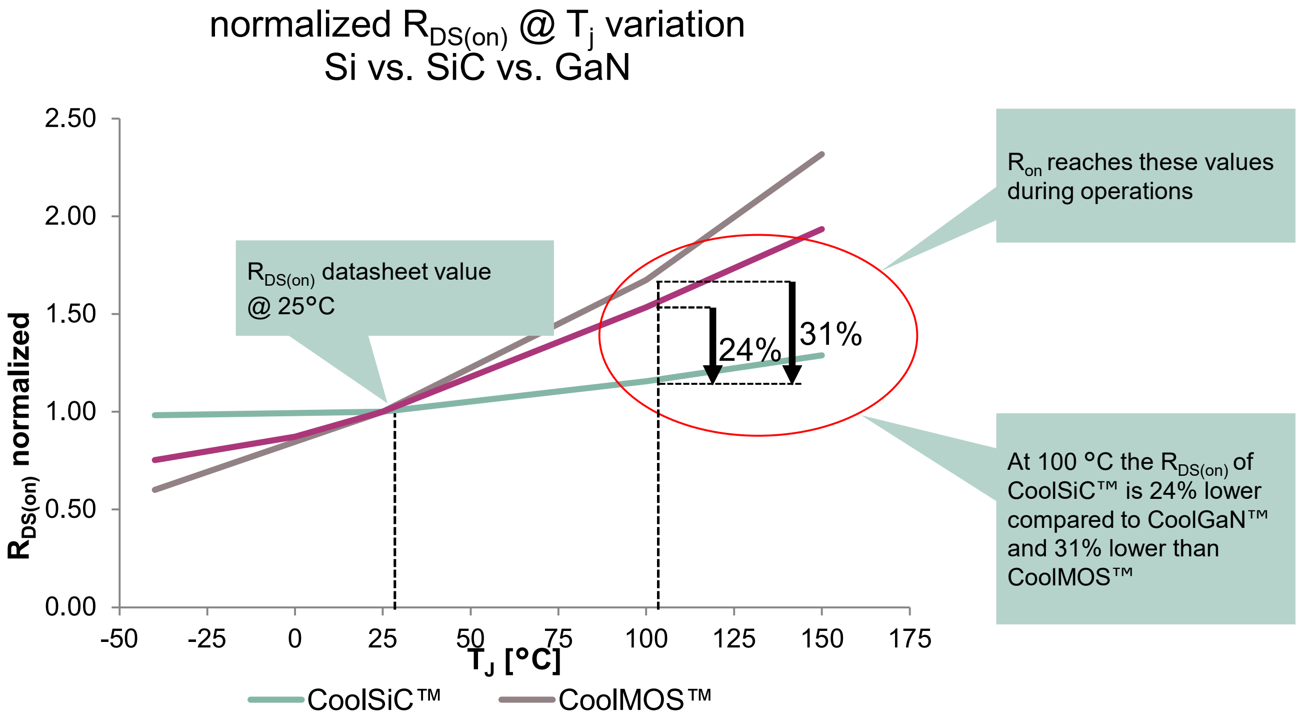


Si Superjunction limit
D. Disney, G. Dolny
ISPSD 2008

CoolSiC™ and CoolGaN™

Thanks to further improvement in manufacturing processes
Si SJ limit potentially pushed lower than 0.5 Ω mm²

Flat temperature dependence of the $R_{DS(on)}$



normalized $R_{DS(on)}$ @ T_j variation
Si vs. SiC vs. GaN

$R_{DS(on)}$ datasheet value @ 25°C

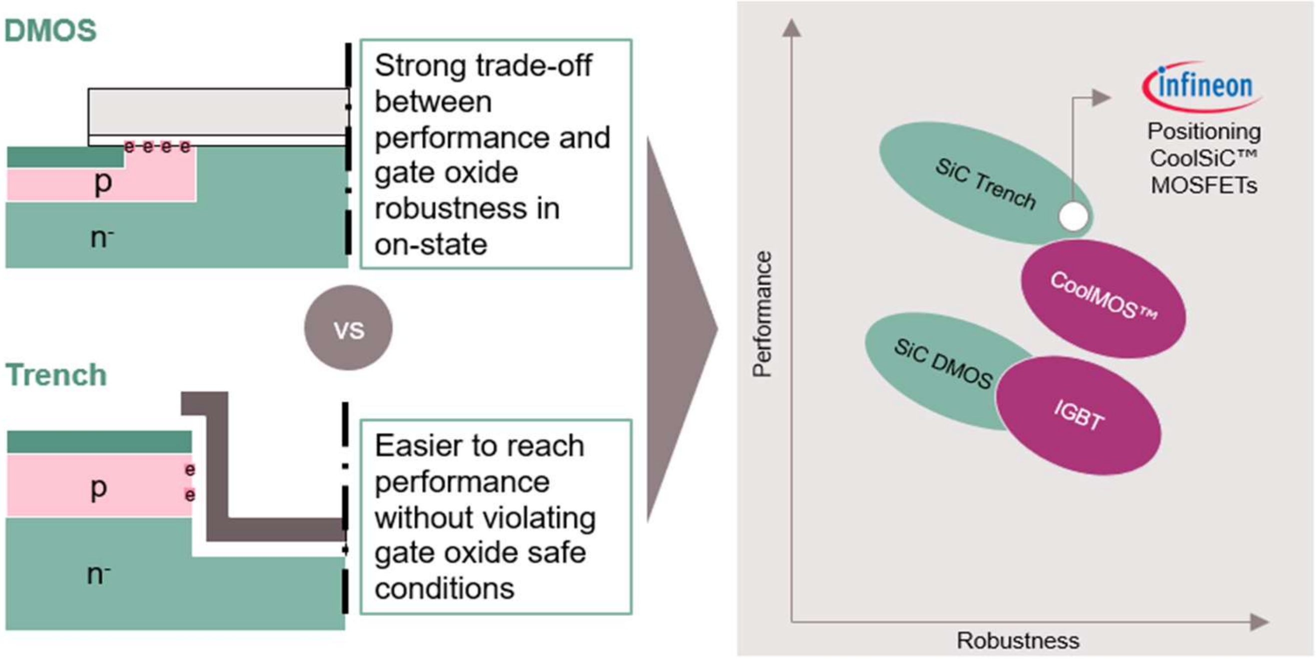
R_{on} reaches these values during operations

At 100 °C the $R_{DS(on)}$ of CoolSiC™ is 24% lower compared to CoolGaN™ and 31% lower than CoolMOS™

- Best dependence of $R_{DS(on)}$ with temperature: allows the use of lower-cost higher $R_{DS(on)}$
- Best thermal conductivity: allows operating at high temperatures

Trench vs. planar: gate oxide reliability and performance

- High defect density leads to high channel resistance and large $R_{ds(on)}$ contribution on the planar architecture
- Vertical SiC interface: low defect density and possible to reach low $R_{ds(on)}$ also with thick GOX
- Thick GOX, low Ron*A, high $V_{gs(th)}$, can therefore be optimized on more attractive level than planar SiC MOSFETs

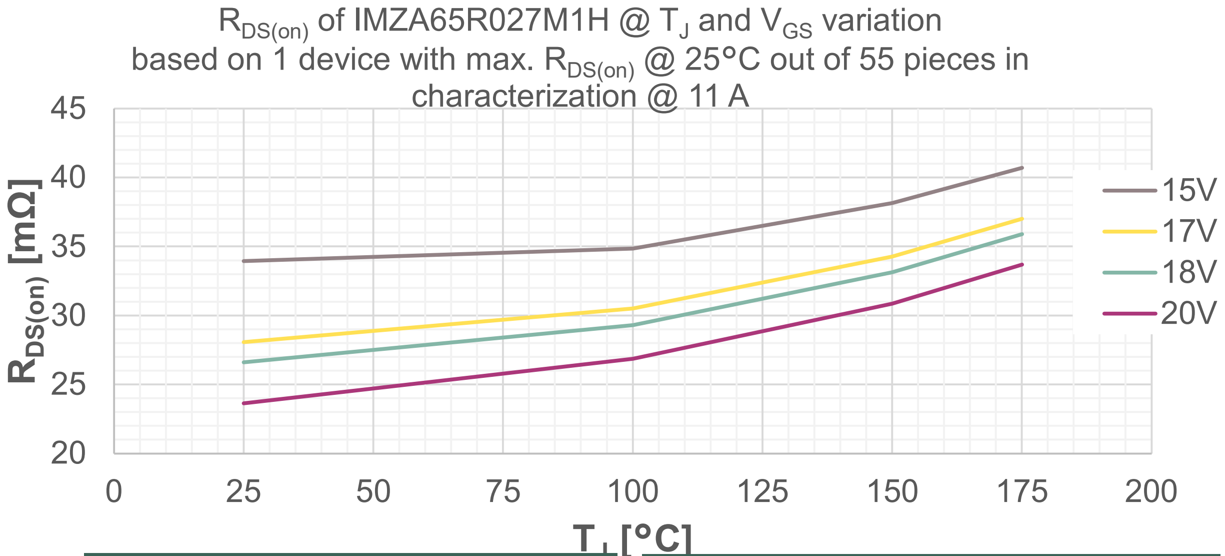


Strong trade-off between performance and gate oxide robustness in on-state

Easier to reach performance without violating gate oxide safe conditions

Positioning CoolSiC™ MOSFETs

Driving voltage: the CoolSiC™ V_{GS} advantage



$R_{DS(on)}$ of IMZA65R027M1H @ T_J and V_{GS} variation
based on 1 device with max. $R_{DS(on)}$ @ 25°C out of 55 pieces in characterization @ 11 A

Recommended $V_{GS(on)}$ = 0 – 18 V (max. 23 V)

- Highest power handling capability through lower $R_{DS(on)}$
- More safety margin against overshoots

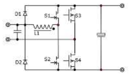
$V_{GS(off)}$ = 0 V

- Enables system simplification in supply voltage and gate drive circuit
- Behaves like CoolMOS™
- Protects against unwanted R_{on} drift

600V/650V CoolMOS™, CoolSiC™, and CoolGaN™ FOMs analysis

DEVICE	$V_{(BR)DSS}$ [V]	$R_{DS(on)}*Q_{rr}$ [mΩ * µC]	$R_{DS(on)}*E_{oss}$ [mΩ * µJ]	$R_{DS(on)}*Q_g$ [mΩ * nC]	$R_{DS(on)}*Q_{os}$ [mΩ * µC]
CoolMOS™ 7	600	100%	100%	100%	100%
CoolMOS™ 7– fast diode	600	10%	104%	108%	104%
CoolGaN™ Gen 1	600	0%	84%	6%	13%
CoolSiC™ Gen 1	650	2%	133%	41%	21%

Allows WBG usage in topologies with repetitive hard commutation (e.g., CCM totem-pole PFC) → BOM savings for highest efficiency

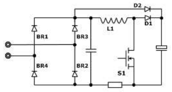


CCM PFC totem-pole

SiC/GaN in servers, OBC

Both SiC and Gan allow an easier way than Si to top efficiency

Minimum switching losses in hard-switching topologies (e.g., classic boost PFC) → higher efficiency with GaN



Classic Boost PFC

Si for best cost – performance ratio

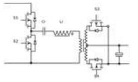
The 3 poducts have similar behaviour in hard-switching topologies like classic PFC

Reduced driving losses especially at light-load conditions. Allows WBG to reach higher efficiency at increased frequency → power density increase (weight & size reduction)

High power density e.g., GaN for chargers

For power density, SiC is better than Si but the champion is GaN

Enables better soft-switching (e.g. half-bridge LLC), where WBG leads to higher efficiency combined with high frequencies

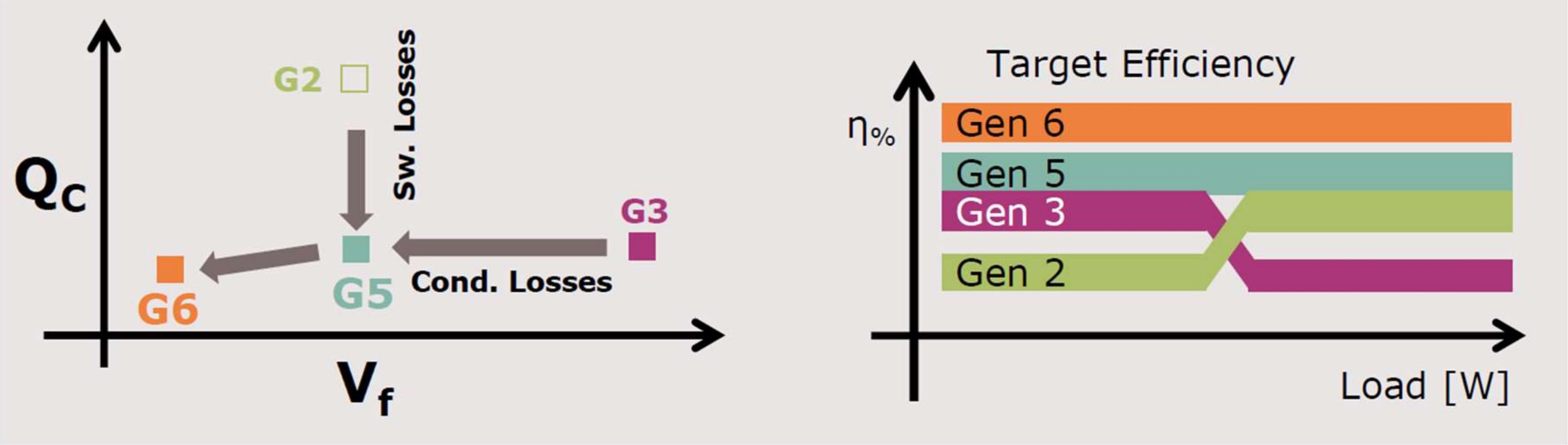


Half-bridge LLC

SiC and GaN e.g., in telecom

SiC and GaN are both better than Si to reach both high efficiency and high density

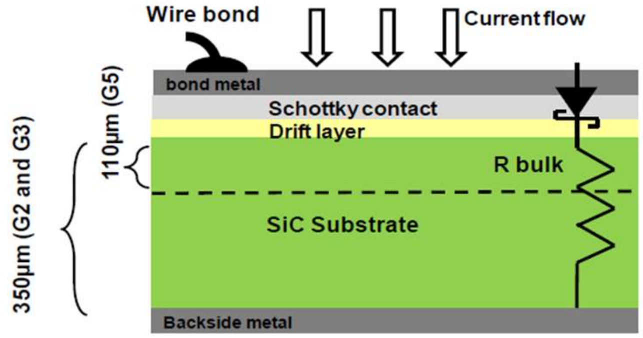
Infineon CoolSiC ™ 650V Gen6 SiC diode Lowest Figure of Merit V_F x Q_C



- **17% FOM Reduction V_f x Q_C** compared to Gen5

→ enabling efficiency benefits over whole load range

ThinQ!TM Technology

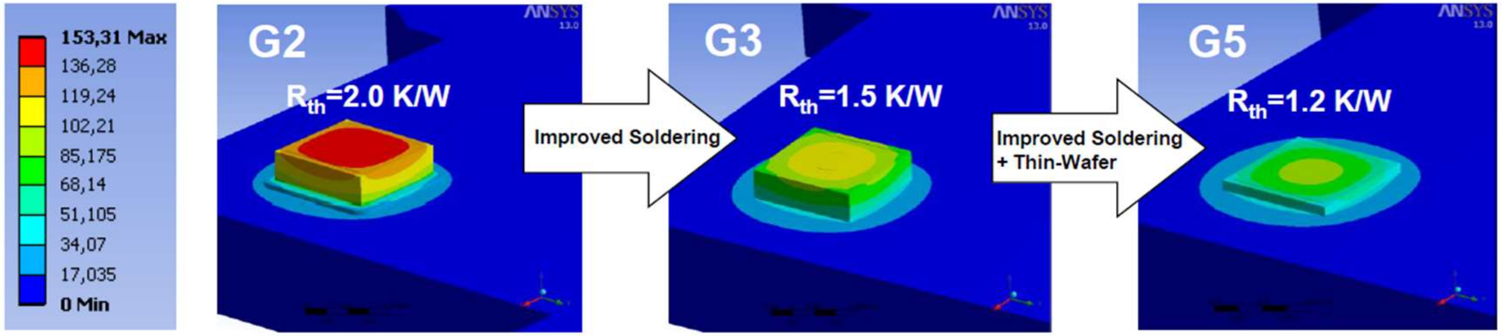


- Reduced substrate thickness
- Patented Diffusion Soldering

⇩

- Better heat spread through lead-frame
- Lower chip temperature
- Lower losses

- Thermal simulation: Equal sized chips in TO-220, P_{loss}=75W



4 英飛淩 CoolSiC™ 產品應用優勢與方案介紹

Si, SiC, and GaN Value proposition in the 600V and 650V segment

Silicon (Si)

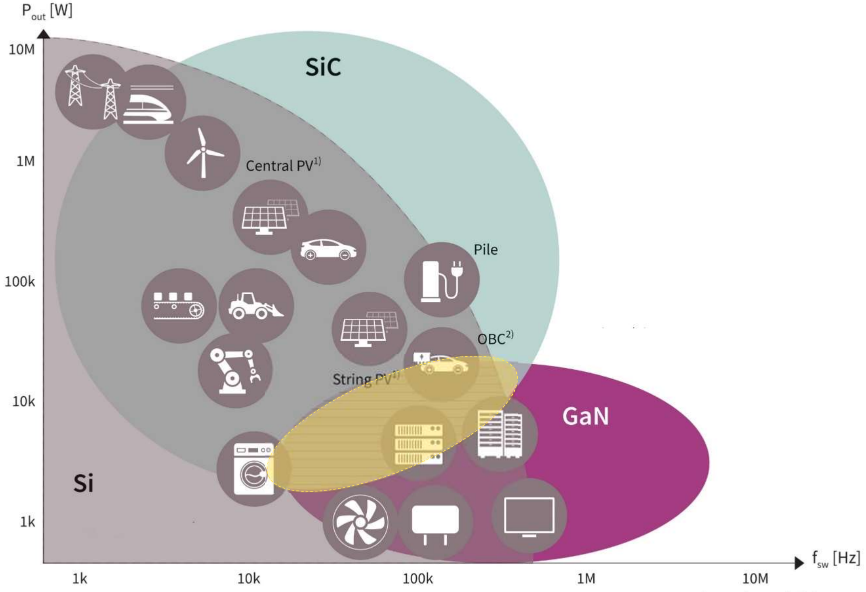
- Targeting voltages ranging from 25 V – 1.7kV
- The mainstream technology
- Suitable from low to high power

Silicon carbide (SiC)

- Targeting voltages ranging from 650 V – 3.3 kV
- High power from moderate to high switching frequency

Gallium nitride (GaN)

- Targeting voltages ranging from 80 V – 650 V
- Medium power at highest switching frequency



1) PV = photovoltaic inverter
2) OBC = on-board charger

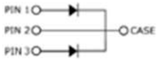
600 V / 650 V segment

CoolMOS™, CoolSiC™, and CoolGaN™ set industry technology benchmark to address any applications with pioneering performance: Datacenter and telecom SMPS, Industrial SMPS, solar inverters, energy storage, UPS, battery formation, EV-charging plus automotive applications like OBC (on-board charger)

CoolSiC™ Schottky diode 600V / 650V A granular and complete portfolio

Ampere [A]	650V TO-220	650V DDPAK	650V TO-247	650V D²PAK	650V ThinPAK 8x8	650V TO-247 dual die	600V DPAK
2A	IDH02G65C5			IDK02G65C5	IDL02G65C5		
3A	IDH03G65C5			IDK03G65C5			IDD03SG60C
4A	IDH04G65C6	IDDD04G65C6		IDK04G65C5	IDL04G65C5		IDD04SG60C
5A	IDH05G65C5			IDK05G65C5			IDD05SG60C
6A	IDH06G65C6	IDDD06G65C6		IDK06G65C5	IDL06G65C5		IDD06SG60C
8A	IDH08G65C6	IDDD08G65C6		IDK08G65C5	IDL08G65C5		IDD08SG60C
9A	IDH09G65C5			IDK09G65C5			IDD09SG60C
10A	IDH10G65C6	IDDD10G65C6	IDW10G65C5	IDK10G65C5	IDL10G65C5		IDD10SG60C
12A	IDH12G65C6	IDDD12G65C6	IDW12G65C5	IDK12G65C5	IDL12G65C5		IDD12SG60C
16A	IDH16G65C6	IDDD16G65C6	IDW16G65C5				
20A	IDH20G65C6	IDDD20G65C6	IDW20G65C5			IDW20G65C5B*	
24A						IDW24G65C5B*	
30/32A			IDW30G65C5			IDW32G65C5B*	
40A			IDW40G65C5			IDW40G65C5B*	

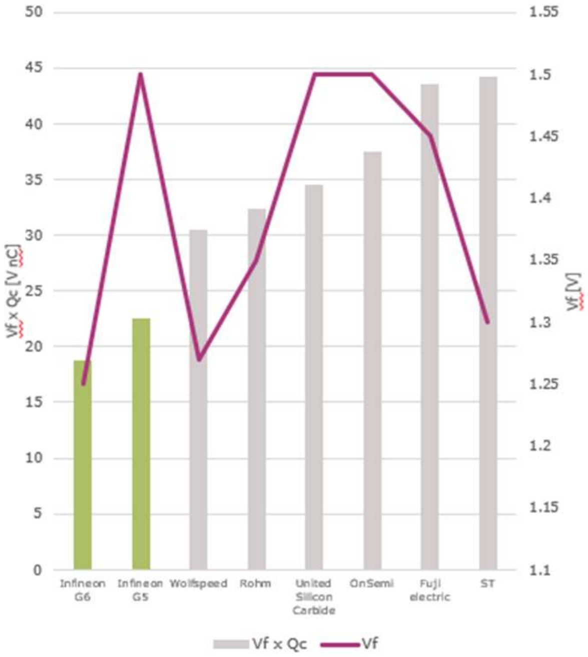
*Common cathode



🟧 G6 products

⬛ G5 products

🟩 G3 products



CoolSiC™ MOSFETs 650 V

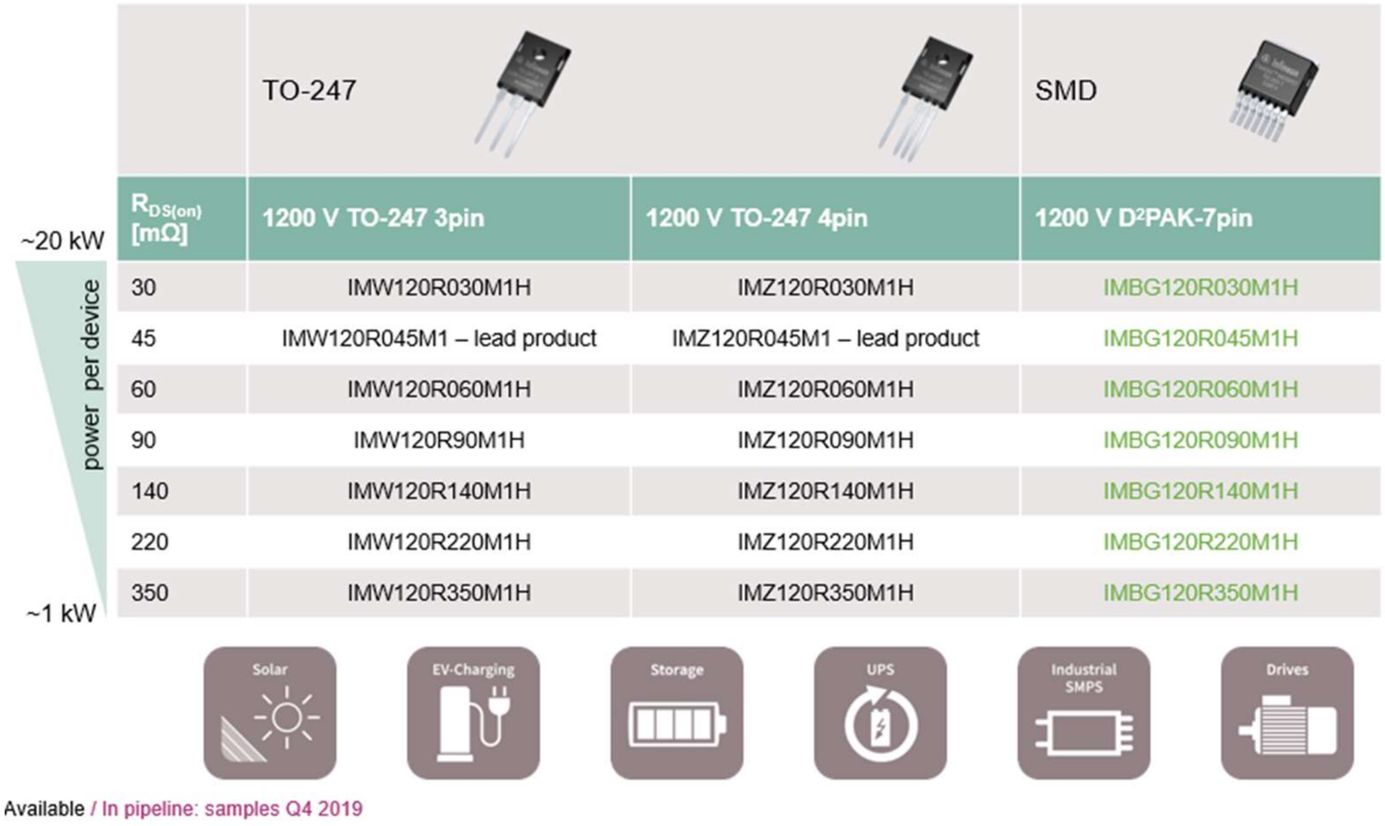
Product portfolio

$R_{DS(on)}$ max [mΩ] 18 V	$R_{DS(on)}$ typ [mΩ] 18 V	TO-247-4 	TO-247-3 
34	27	IMZA65R027M1H	IMW65R027M1H
42	30	IMZA65R030M1H	IMW65R030M1H
50	39	IMZA65R039M1H	IMW65R039M1H
64	48	IMZA65R048M1H	IMW65R048M1H
74	57	IMZA65R057M1H	IMW65R057M1H
94	72	IMZA65R072M1H	IMW65R072M1H
111	83	IMZA65R083M1H	IMW65R083M1H
142	107	IMZA65R107M1H	IMW65R107M1H

Target applications

- Server
- Telecom
- Industrial SMPS
- Solar
- EV-Charging
- UPS
- Battery formation
- Energy storage
- Servo drives
- Motor drivers
- Home Appliance

Broad discrete CoolSiC™ MOSFET 1200 V portfolio for 3-phase power systems in the range of 1 – 80 kW



~20 kW

power per device

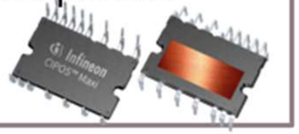
~1 kW

	TO-247		SMD
$R_{DS(on)}$ [mΩ]	1200 V TO-247 3pin	1200 V TO-247 4pin	1200 V D²PAK-7pin
30	IMW120R030M1H	IMZ120R030M1H	IMBG120R030M1H
45	IMW120R045M1 – lead product	IMZ120R045M1 – lead product	IMBG120R045M1H
60	IMW120R060M1H	IMZ120R060M1H	IMBG120R060M1H
90	IMW120R90M1H	IMZ120R090M1H	IMBG120R090M1H
140	IMW120R140M1H	IMZ120R140M1H	IMBG120R140M1H
220	IMW120R220M1H	IMZ120R220M1H	IMBG120R220M1H
350	IMW120R350M1H	IMZ120R350M1H	IMBG120R350M1H

Available / In pipeline: samples Q4 2019

CoolSiC™ MOSFET
Solutions for integrated servo motor for robotics

- **CoolSiC™ IPM – CIPOS™ Maxi**
  - IM828
  - Compact design
  - Integrated driver and protect circuit

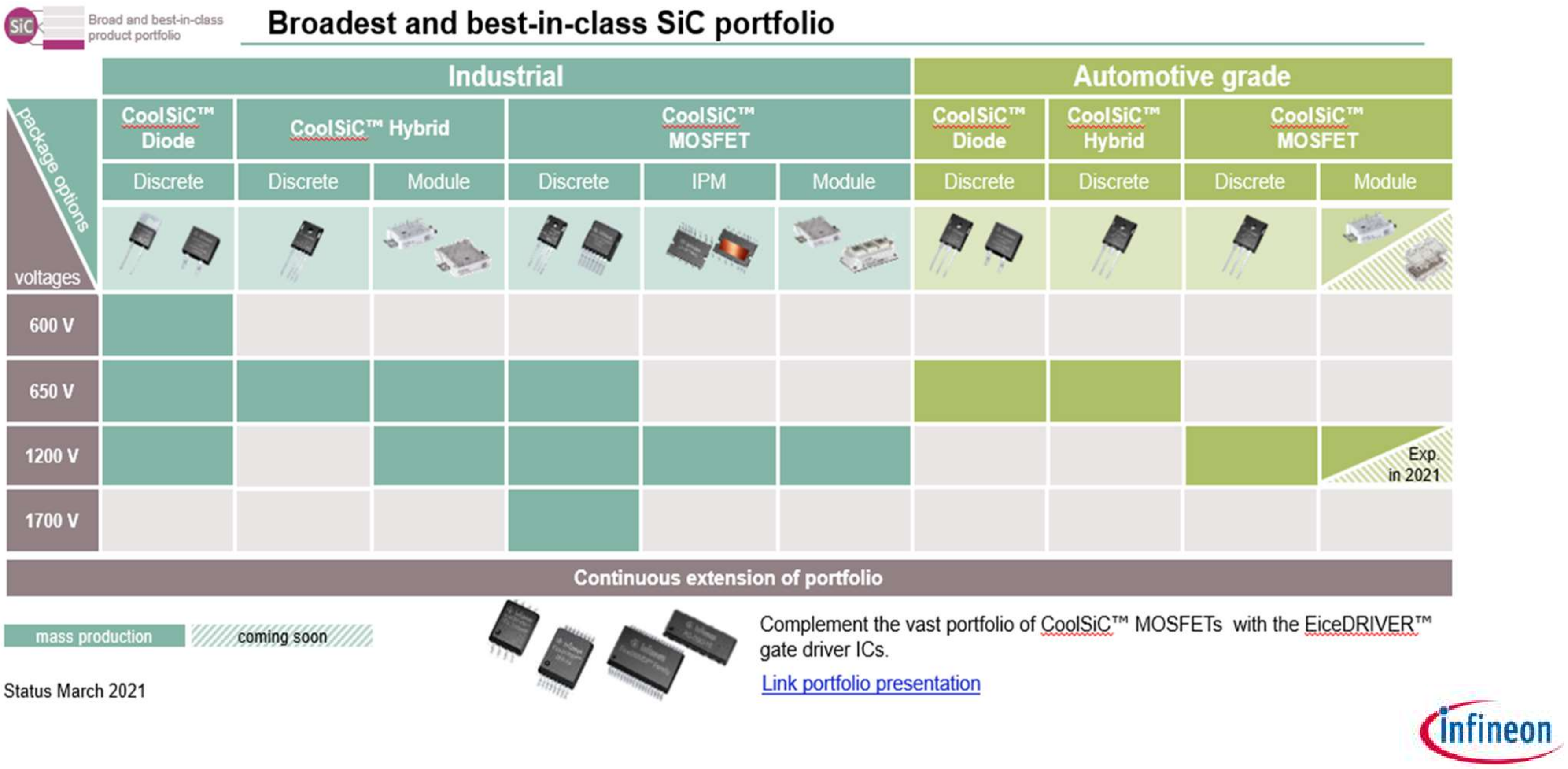


- **CoolSiC™ module – EasyPACK™**
  - FS45MR12W1M1_B11
  - B6 topology with NTC
  - Simple mounting

- **CoolSiC™ discrete – TO-247-3/4**
  - E.g. IMZ120R030M1H
  - Full portfolio 30/60/90/140 mΩ for various drives power classes

- **CoolSiC™ discrete – TO-263-7**
  - IMBG120R030M1H
  - Cooling concept via IMS
    ➔ Good thermal performance
  - Full portfolio 30/60/90/140 mΩ to cover various drives power classes will be available soon

Strong CoolSiC™ portfolio expansion: by packages and by voltages



Broadest and best-in-class SiC portfolio

package options / voltages	Industrial						Automotive grade			
	CoolSiC™ Diode	CoolSiC™ Hybrid		CoolSiC™ MOSFET			CoolSiC™ Diode	CoolSiC™ Hybrid	CoolSiC™ MOSFET	
	Discrete	Discrete	Module	Discrete	IPM	Module	Discrete	Discrete	Discrete	Module
600 V	■									
650 V	■	■	■	■			■	■		
1200 V	■		■	■	■	■			■	■ ▨ Exp. in 2021
1700 V				■						

Continuous extension of portfolio

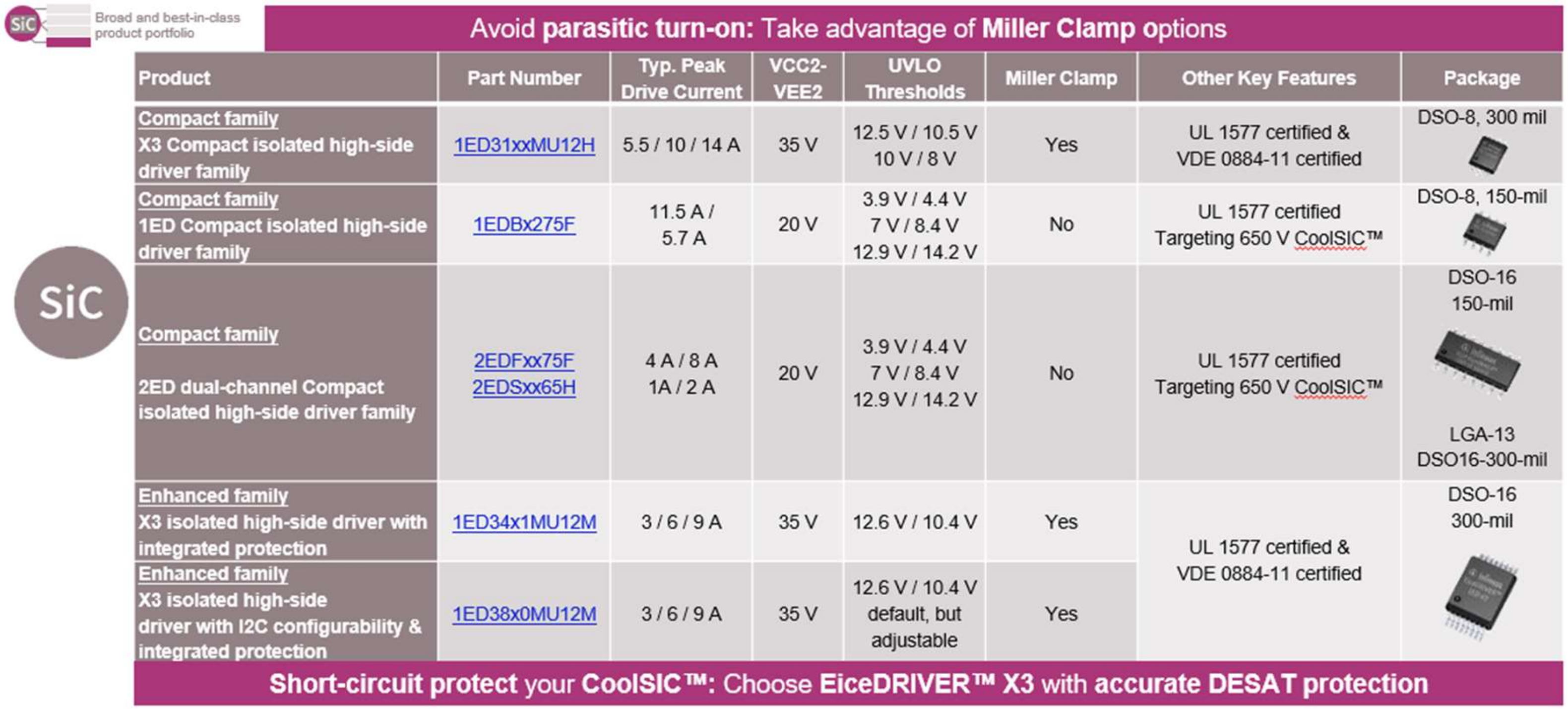
■ mass production
▨ coming soon

Status March 2021

Complement the vast portfolio of CoolSiC™ MOSFETs with the EiceDRIVER™ gate driver ICs.

Link portfolio presentation

CoolSiCEiceDRIVER™ gate driver portfolio forms the perfect match with CoolSiC™

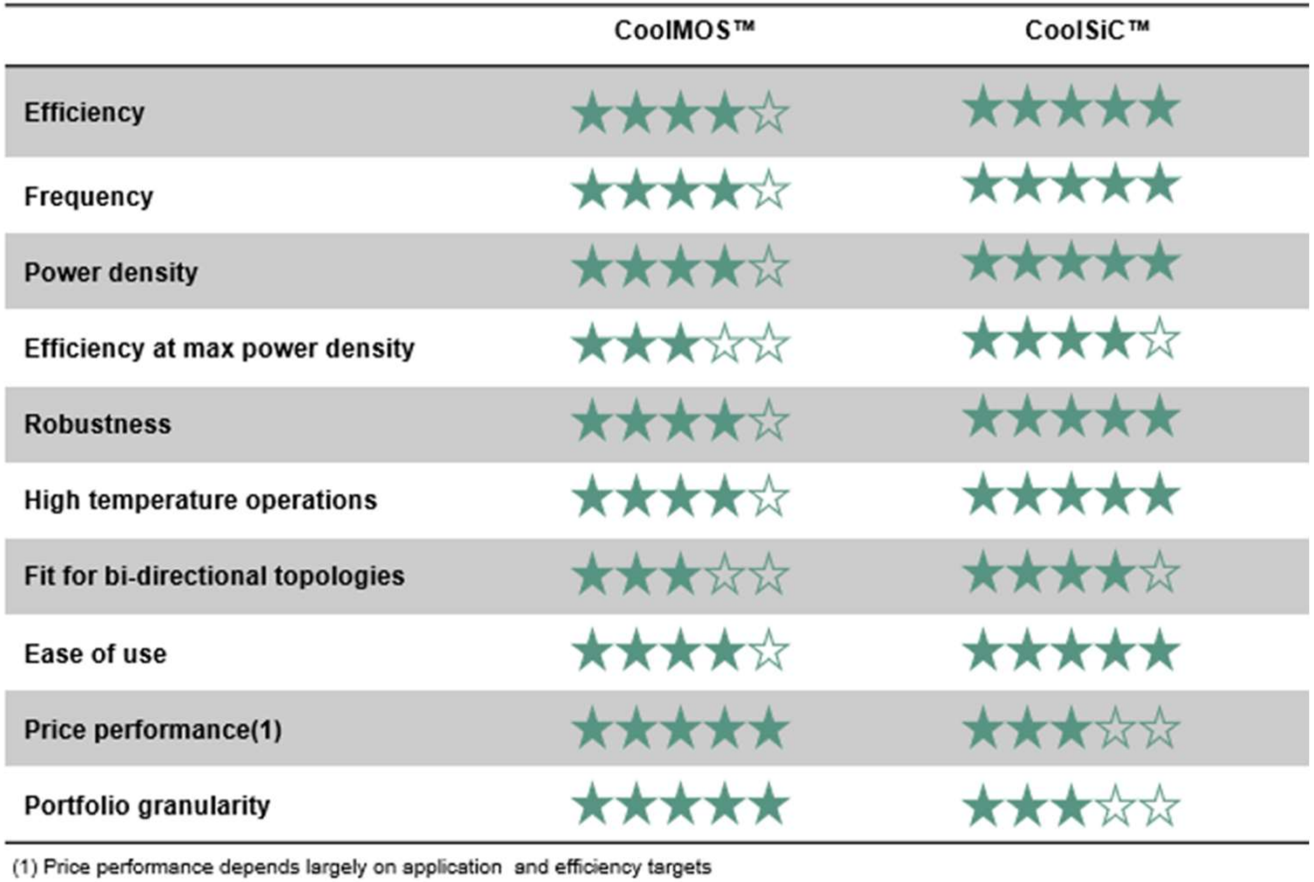


Avoid **parasitic turn-on:** Take advantage of **Miller Clamp** options

Product	Part Number	Typ. Peak Drive Current	VCC2-VEE2	UVLO Thresholds	Miller Clamp	Other Key Features	Package
Compact family X3 Compact isolated high-side driver family	1ED31xxMU12H	5.5 / 10 / 14 A	35 V	12.5 V / 10.5 V 10 V / 8 V	Yes	UL 1577 certified & VDE 0884-11 certified	DSO-8, 300 mil
Compact family 1ED Compact isolated high-side driver family	1EDBx275F	11.5 A / 5.7 A	20 V	3.9 V / 4.4 V 7 V / 8.4 V 12.9 V / 14.2 V	No	UL 1577 certified Targeting 650 V CoolSIC™	DSO-8, 150-mil
Compact family 2ED dual-channel Compact isolated high-side driver family	2EDFxx75F 2EDSxx65H	4 A / 8 A 1A / 2 A	20 V	3.9 V / 4.4 V 7 V / 8.4 V 12.9 V / 14.2 V	No	UL 1577 certified Targeting 650 V CoolSIC™	DSO-16 150-mil LGA-13 DSO16-300-mil
Enhanced family X3 isolated high-side driver with integrated protection	1ED34x1MU12M	3 / 6 / 9 A	35 V	12.6 V / 10.4 V	Yes	UL 1577 certified & VDE 0884-11 certified	DSO-16 300-mil
Enhanced family X3 isolated high-side driver with I2C configurability & integrated protection	1ED38x0MU12M	3 / 6 / 9 A	35 V	12.6 V / 10.4 V default, but adjustable	Yes		

Short-circuit protect your **CoolSIC™:** Choose **EiceDRIVER™ X3** with **accurate DESAT protection**

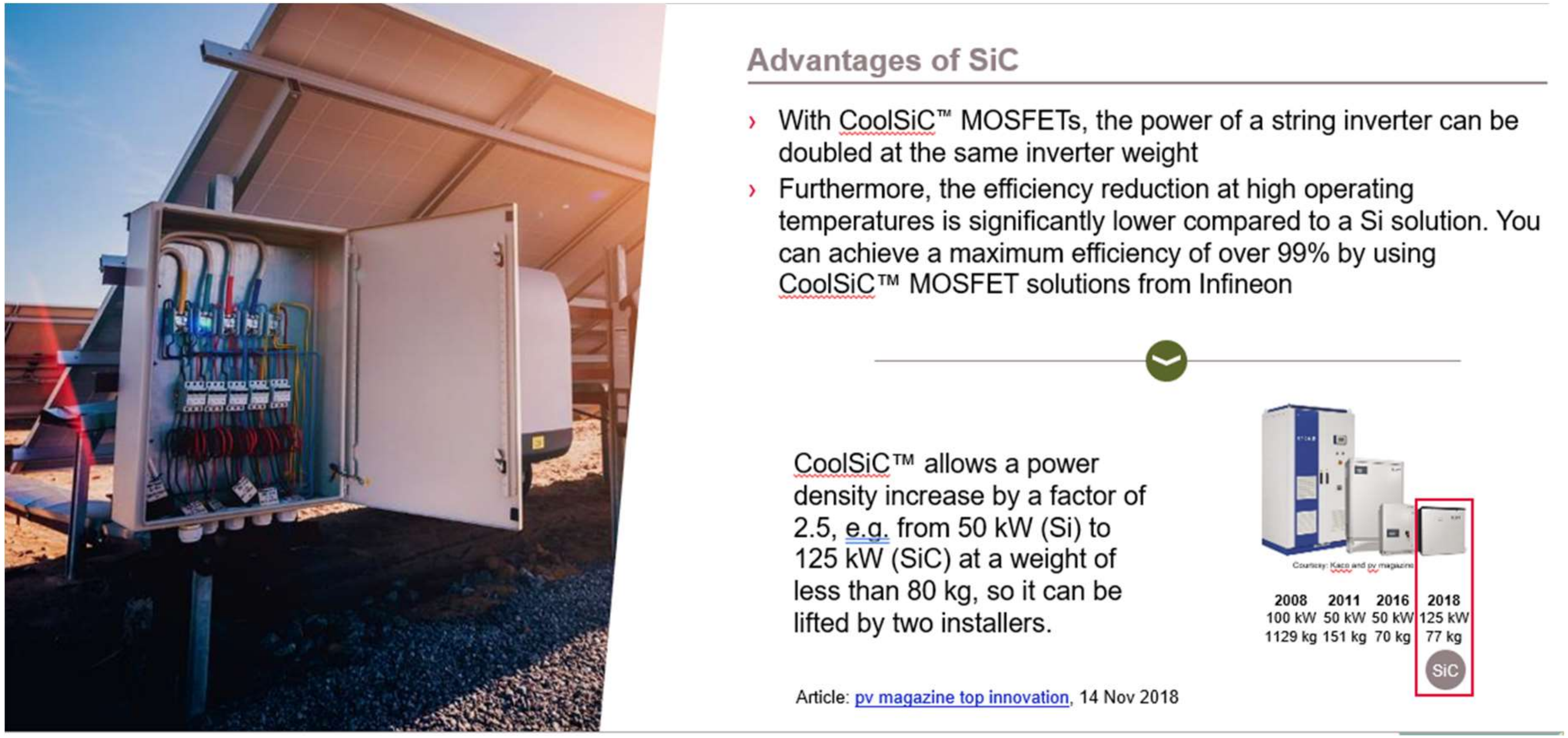
SiC and Si positioning – summary



	CoolMOS™	CoolSiC™
Efficiency	★★★★☆	★★★★★
Frequency	★★★★☆	★★★★★
Power density	★★★★☆	★★★★★
Efficiency at max power density	★★★☆☆	★★★★☆
Robustness	★★★★☆	★★★★★
High temperature operations	★★★★☆	★★★★★
Fit for bi-directional topologies	★★★☆☆	★★★★☆
Ease of use	★★★★☆	★★★★★
Price performance(1)	★★★★★	★★★☆☆
Portfolio granularity	★★★★★	★★★☆☆

(1) Price performance depends largely on application and efficiency targets

Solar string inverters are strongly benefitting from the advantages that CoolSiC™ MOSFETs provide



Advantages of SiC

- With CoolSiC™ MOSFETs, the power of a string inverter can be doubled at the same inverter weight
- Furthermore, the efficiency reduction at high operating temperatures is significantly lower compared to a Si solution. You can achieve a maximum efficiency of over 99% by using CoolSiC™ MOSFET solutions from Infineon

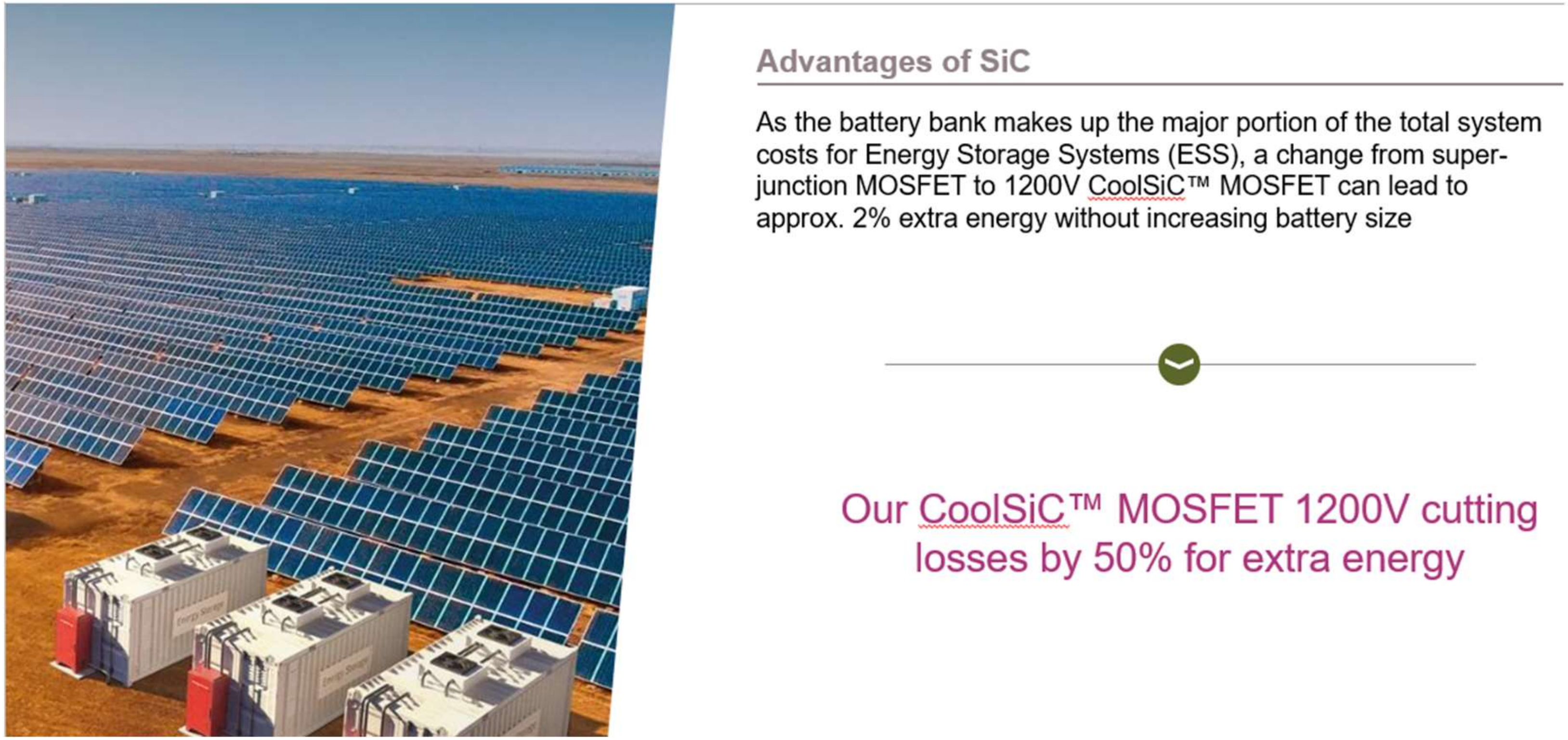
CoolSiC™ allows a power density increase by a factor of 2.5, e.g. from 50 kW (Si) to 125 kW (SiC) at a weight of less than 80 kg, so it can be lifted by two installers.

Courtesy: Kaco and pv magazine

2008	2011	2016	2018
100 kW	50 kW	50 kW	125 kW
1129 kg	151 kg	70 kg	77 kg
			SiC

Article: pv magazine top innovation, 14 Nov 2018

CoolSiC™ helps to reduce energy losses leading to some extra energy, available when needed



Advantages of SiC

As the battery bank makes up the major portion of the total system costs for Energy Storage Systems (ESS), a change from super-junction MOSFET to 1200V CoolSiC™ MOSFET can lead to approx. 2% extra energy without increasing battery size

Our CoolSiC™ MOSFET 1200V cutting losses by 50% for extra energy

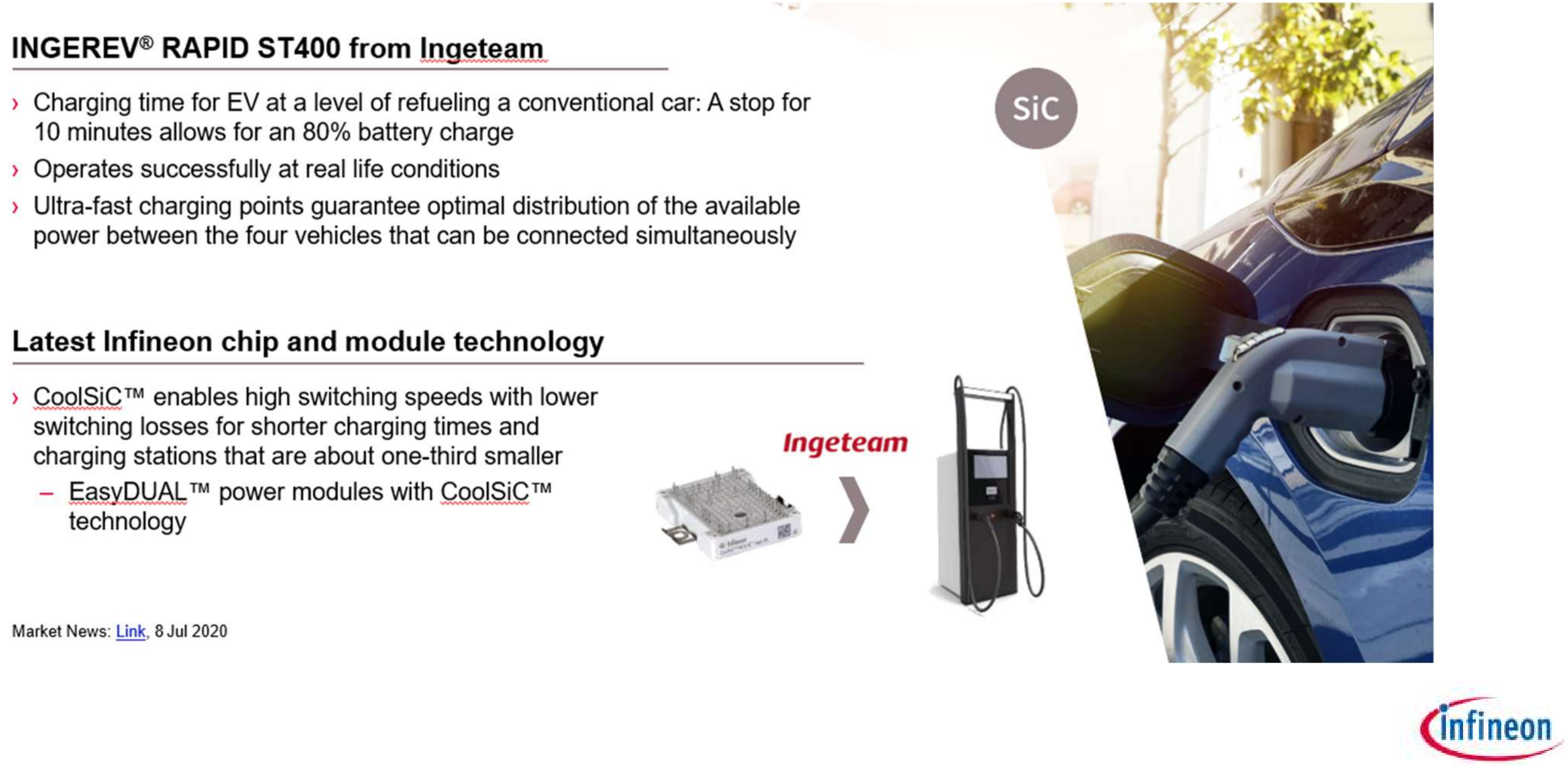
CoolSiC™ enables reduction of system size of Industrial Power Supply applications

Advantages of SiC

- CoolSiC™ MOSFET offers highest efficiency, and cuts energy losses by half in the 24/7 operation of online UPS systems
- Number of heat sinks and filters can be reduced, thus decreasing the system size and the space required
- By reaching highest efficiency levels, you can lower cooling requirements and keep your maintenance and servicing costs low

Using CoolSiC™ MOSFETs in a high-power UPS will improve the Total Cost of Ownership (TCO) significantly.

Europe's most powerful 400 kW DC charger: CoolSiC™ for ultra-fast pit stops



INGEREV® RAPID ST400 from Ingeteam

- Charging time for EV at a level of refueling a conventional car: A stop for 10 minutes allows for an 80% battery charge
- Operates successfully at real life conditions
- Ultra-fast charging points guarantee optimal distribution of the available power between the four vehicles that can be connected simultaneously

Latest Infineon chip and module technology

- CoolSiC™ enables high switching speeds with lower switching losses for shorter charging times and charging stations that are about one-third smaller
  - EasyDUAL™ power modules with CoolSiC™ technology

Market News: Link, 8 Jul 2020

CoolSiC™ MOSFET powers the next generation of servo drives design

Advantages of SiC

- Up to 80% of total loss reduction is enabled by more than 50% switching loss reduction
- 80% reduction of low current conduction loss by resistive behavior
- CoolSiC™ enables motor and drive integration and hence, reduces the complexity of cabling

No more need for a cooling fan since passive cooling is sufficient, therefore reducing your maintenance effort to a minimum.

CoolSiC™ in Server and Telecom power: A simpler way to very high efficiency

Advantages of SiC

- Supports 50% reduction of losses
- Doubling of power density
- Simplified and cost effective design for top efficiency systems
- Enablement of high power fanless designs for 5G deployment

CoolSiC™ MOSFET 650V enables the cost effective design of top efficiency and density SMPS

Thank You

Questions

AVNET® 100 YEARS

Reach Further® Together

Gate Driver Design for SiC & Success Stories

09.01.2021 **Sam Tseng**, Field Application Engineer

Agenda

1 Gate driver design

2 Success Stories

Gate Driver Design

Gate driver design

1 SiC MOSFETs characteristics & Gate driver IC

2 Gate driver design step-by-step

SiC MOSFETs Main characteristics

Fast switching devices

✓ Can reach ≥ 50 V/ns

IGBT-dominated working environment:
each mm of PCB track has a strong influence on the MOSFETs' switching performance due to high di/dt

SiC MOSFETs Main characteristics

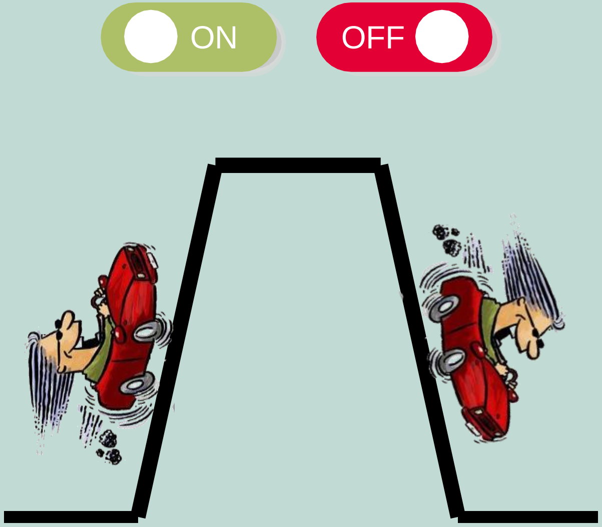
Fast switching devices

- ✓ Can reach ≥ 50 V/ns

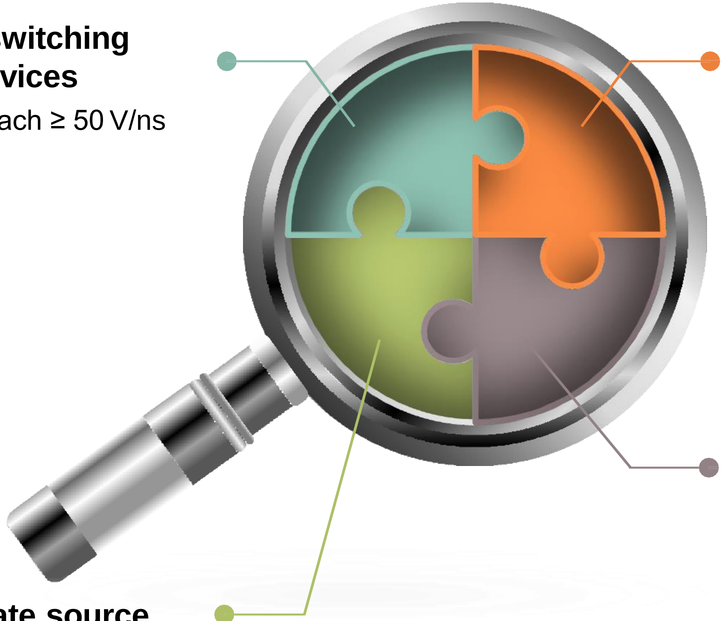
MOSFET-driven working environment:
higher DC-link voltages lead to longer exposure of the gate driver IC to common mode transients

SiC MOSFETs Main characteristics

Fast switching enables high switching frequencies



SiC MOSFETs Main characteristics



Fast switching devices

✓ Can reach ≥ 50 V/ns

Lower reverse recovery charge

✓ Freewheeling body diode with little Q_r, but with high VF

On-state performance

✓ Short circuit performance scarified

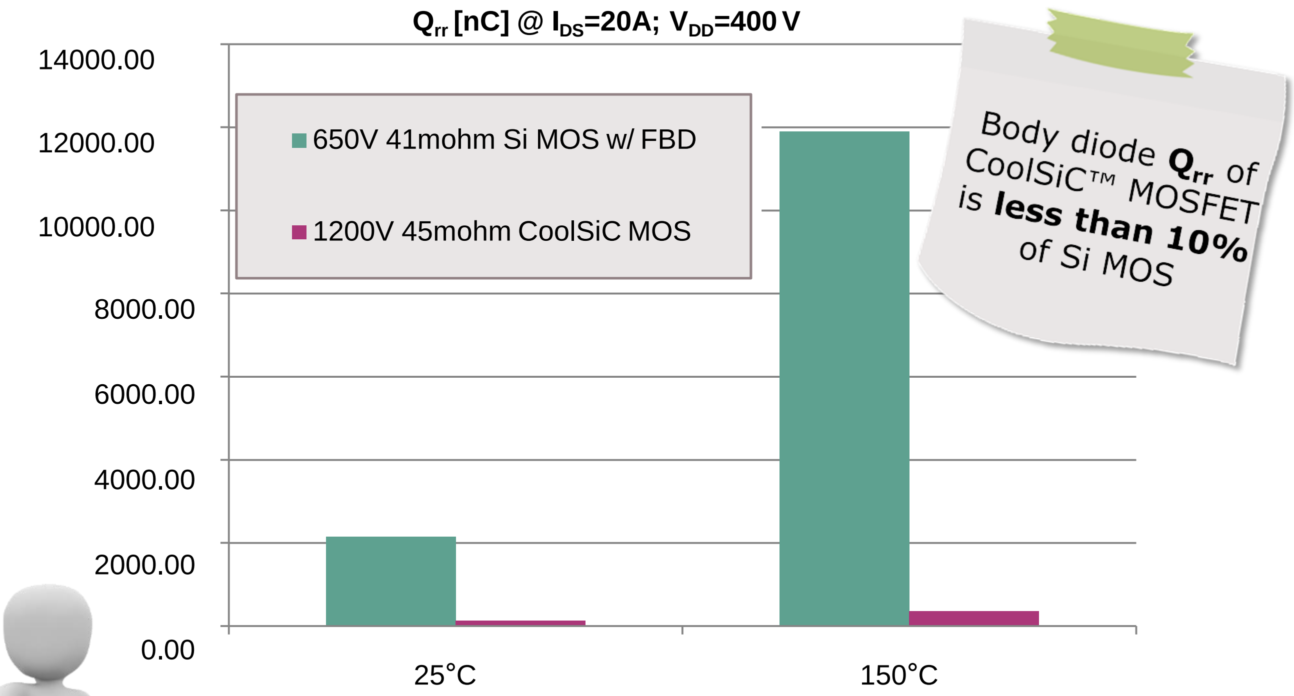
High-gate source voltage

✓ May need a negative gate voltage to stay in off-mode

Gate driver circuits and ICs should support all these characteristics!

Reverse recovery charge Q_{rr} of body diode

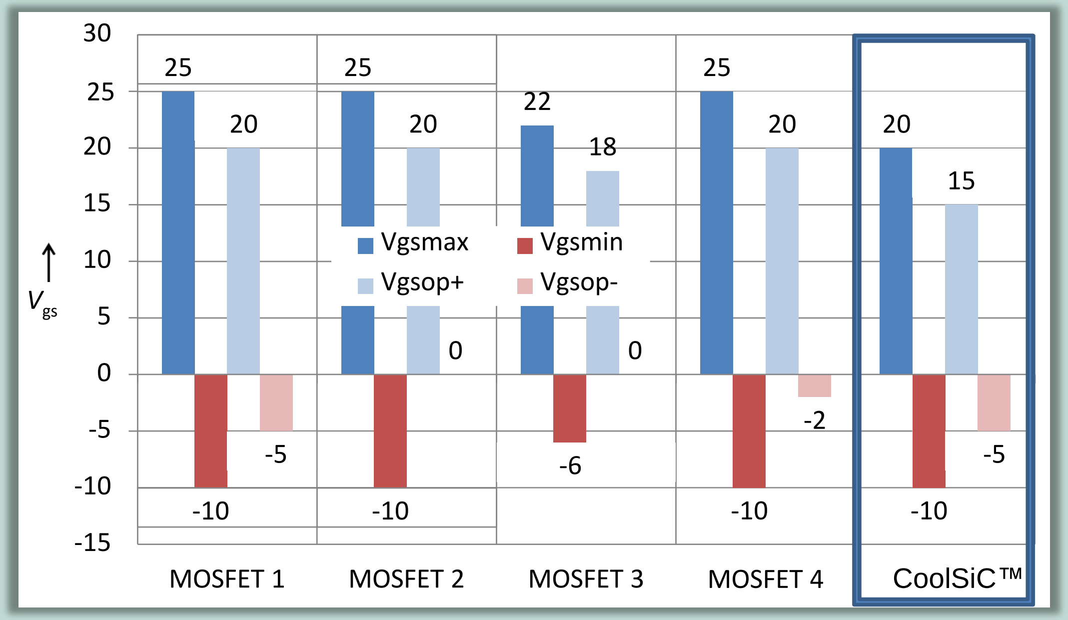
- Si MOS vs SiC MOS



Body diode **Q_{rr}** of CoolSiC™ MOSFET is **less than 10%** of Si MOS

CoolSiC™ MOSFET has much lower Q_{rr}
that can operate with higher switching frequency!

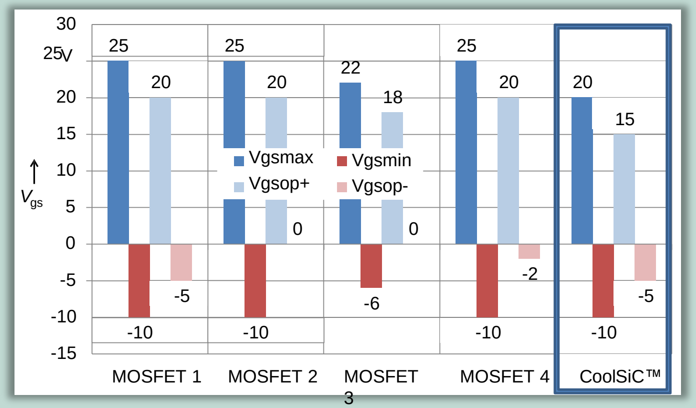
Market-relevant SiC MOSFETs



🟥 🟦 *Max. gate-source voltage range*

▨ ▨ *Operating gate-source voltage range*

Market-relevant SiC MOSFETs

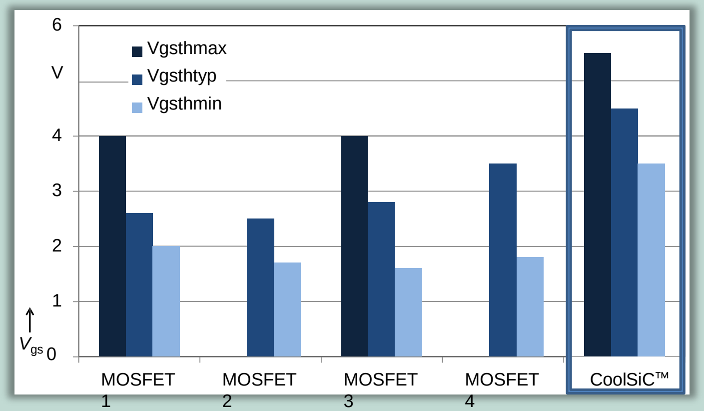


- Operating range:
  - considerably higher than IGBTs
  - even higher than silicon MOSFETs
- Supply capability of at least 25 – 30 V is recommended for driver ICs

↓

Infineon's CoolSiC™ technology offers the advantage of requiring +15 V only!

Negative gate voltage



Using negative gate voltage is state-of-the-art to avoid parasitic dv/dt-triggered turn-on!

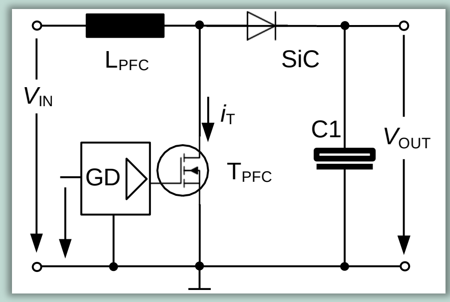
- SiC MOSFETs have lower gate-source threshold voltage than IGBTs or silicon MOSFETs
- CoolSiC™: $V_{gs(th)} = 4.5$ V
- Still prone to parasitic dV_{DS}/dt turn-on

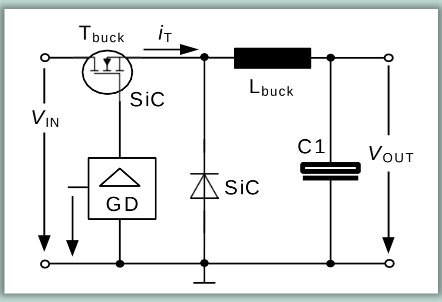
↓

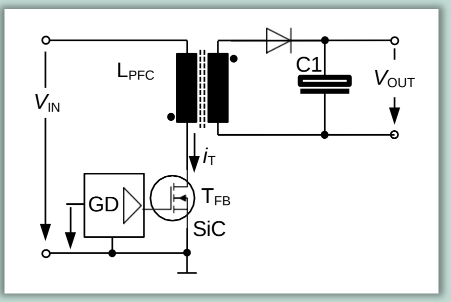
Minor negative gate voltage of $-5\text{ V} < V_{gs,neg} < 0$ strongly recommended during turn-off

Single transistor topologies

Switch mode power supplies with a single power transistor use mainly 0 – 15 V gate supply



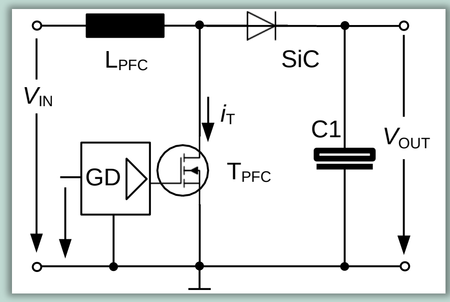


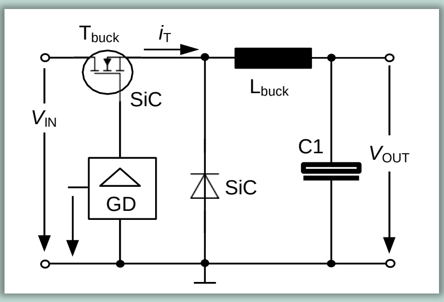


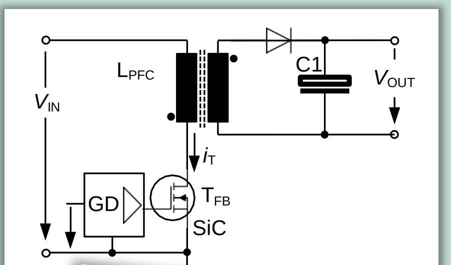
- Passive dv/dt events do not occur during off-state
- Threat of parasitic dV_{DS}/dt-triggered turn-on reduced

Single transistor topologies

Switch mode power supplies with a single power transistor use mainly 0 – 15 V gate supply







Active miller clamp function can support off-state mode at a gate-source voltage of 0 V

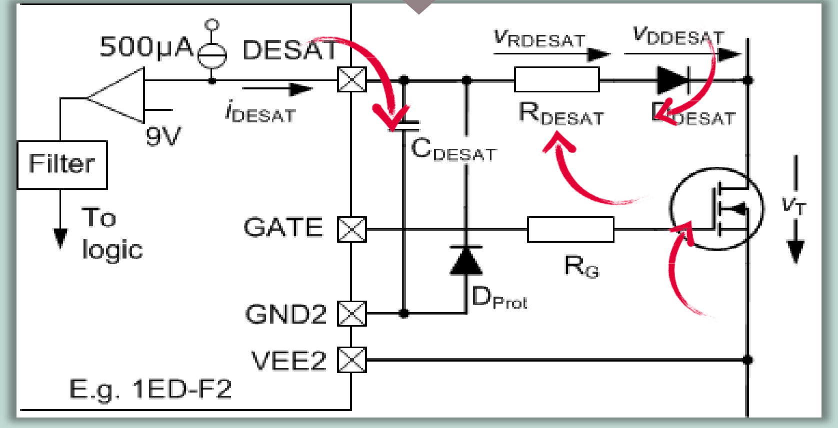
EiceDRIVER™ ICs with active miller clamp and unipolar gate supply can be sufficient

Short circuit performance

- SiC MOSFETs have minor or even no short circuit capability
- Only CoolSiC™ is short circuit rated (max.: 3 µs)

DESAT function

Short circuit detection



Formula

$$v_{T,trig} = 9\ V - v_{RDESAT} - v_{DDESAT}$$

$$= 9\ V - 500\ \mu A \cdot R_{DESAT} - 0.7\ V$$

- DESAT-to-shutdown delay: 430 ns max.
- IC should be triggered at $V_T = 2 - 4$ V
- Tuning for DESAT trigger:
  - a higher value for R_{DESAT} (e.g. 10 kΩ)
  - Zener diode in series to R_{DESAT}

EiceDRIVER™ ICs DESAT parameters

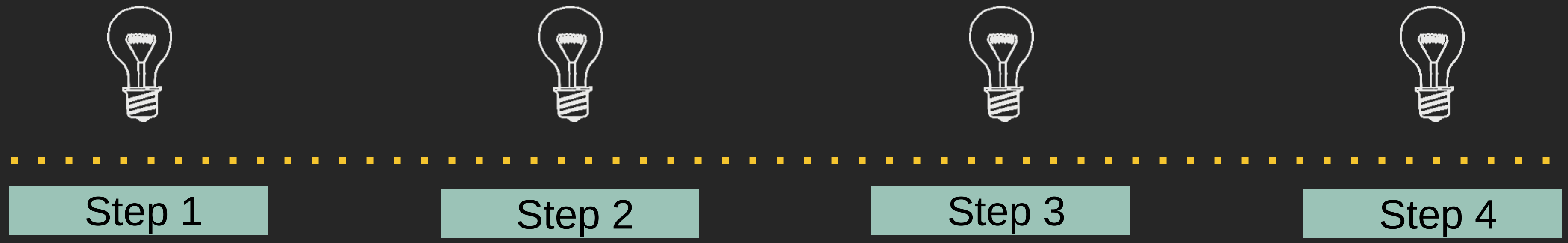
EiceDRIVER™ sales code x = “F” or “H” (package options)	Typ. I_{DESAT}	Typ. V_{DESAT}	Max. T_{DESAT}
1ED020I12-F2 / ED020I12-B2 **2ED020I12-F2**	500 µA	9 V	430 ns
1EDI20I12SV / 1EDU20I12SV **1EDS20I12SV**	500 µA	9 V	540 ns

Gate driver design

1 SiC MOSFETs characteristics & Gate driver IC

2 Gate driver design step-by-step

Design steps



Step 1

Step 2

Step 3

Step 4

Design steps may be fully iterated or partially iterated until the final selection is done

Design steps

Calculate peak I_g based on the power transistor’s datasheet
Select suitable gate driver based on peak current

Step 1

Peak current
and gate
driver IC
selection

Step 2

Step 3

Step 4

Design steps

Calculate gate resistor based on your application’s gate voltage swing
Target: get the same switching performance as in datasheet

Step 1

Peak current and gate driver IC selection

Step 2

Adaptation of gate resistor value to the application conditions

Step 3

Step 4

Design steps

Calculate internal power dissipation of the IC Calculate the gate resistor’s power dissipation

Verify both power dissipations with datasheet values

Step 1

Peak current and gate driver IC selection

Step 2

Adaptation of gate resistor value to the application conditions

Step 3

Power dissipation

Step 4

Design steps

Validate absence of oscillations and parasitic turn-on
Verify thermal behavior of gate driver IC in the application

Step 1

Peak current and gate driver IC selection

Step 2

Adaptation of gate resistor value to the application conditions

Step 3

Power dissipation

Step 4

Laboratory validation

Design steps

If in step 4 results are not as expected - iteration loops may occur

Step 1

Peak current and gate driver IC selection

Step 2

Adaptation of gate resistor value to the application conditions

Step 3

Power dissipation

Step 4

Laboratory validation

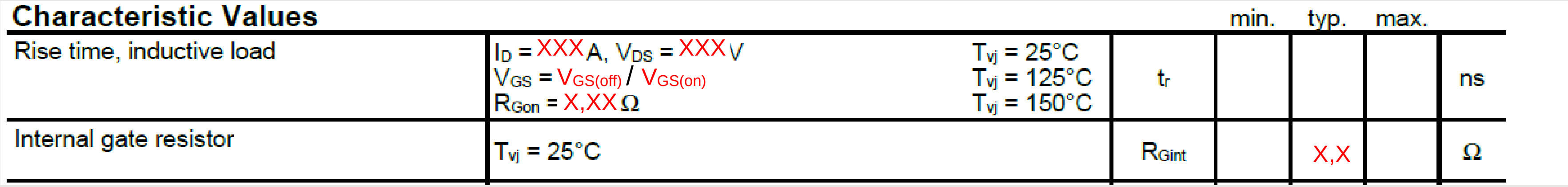
Step 1:Calculation of IG and selection of gate driver IC

$$I_G = \frac{\Delta V_{GS,\text{datasheet}}}{R_{G,\text{datasheet}} + R_{G,\text{int}}}$$

This formula ignores the internal resistance of the selected gate driver

Step 1:Calculation of IG and selection of gate driver IC

$$I_{\mathrm{G}} = \frac{\Delta V_{\mathrm{GS,datasheet}}}{R_{\mathrm{G,datasheet}} + R_{\mathrm{G,int}}}$$

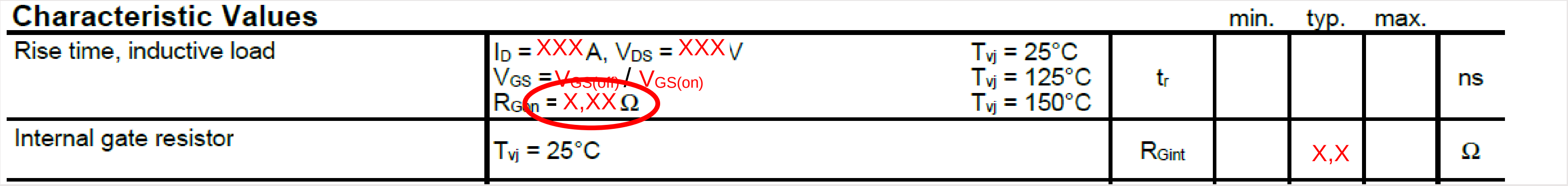


Characteristic Values				min.	typ.	max.	
Rise time, inductive load	I_D = XXX A, V_{DS} = XXX V V_{GS} = $V_{GS(off)}$ / $V_{GS(on)}$ R_{Gon} = X,XX Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	t_r				ns
Internal gate resistor	T_{vj} = 25°C		R_{Gint}		X,X		Ω

This formula ignores the internal resistance of the selected gate driver

Step 1:Calculation of IG and selection of gate driver IC

$$I_G = \frac{\Delta V_{GS,datasheet}}{R_{G,datasheet} + R_{G,int}}$$



Characteristic Values

				min.	typ.	max.	
Rise time, inductive load	I_D = XXX A, V_{DS} = XXX V V_{GS} = $V_{GS(off)}$ / $V_{GS(on)}$ R_{Gon} = X,XX Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	t_r				ns
Internal gate resistor	T_{vj} = 25°C		R_{Gint}		X,X		Ω

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Step 1:Calculation of IG and selection of gate driver IC

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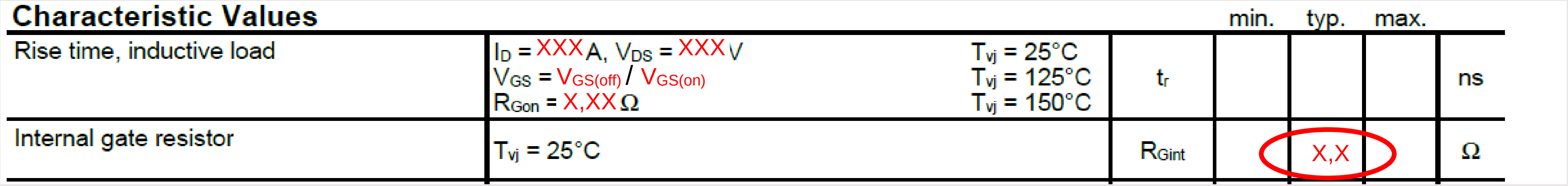


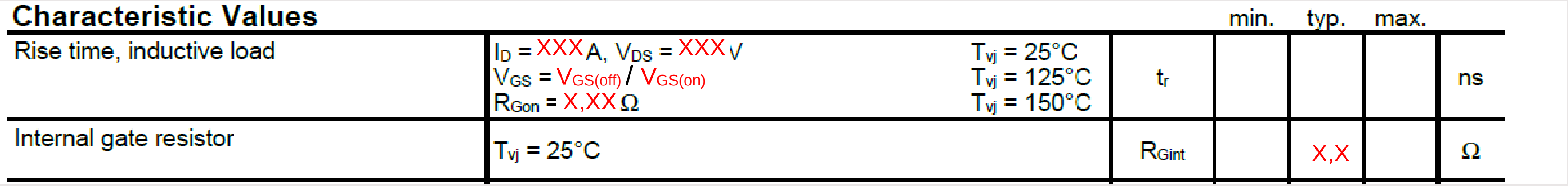
Characteristic Values				min.	typ.	max.	
Rise time, inductive load	I_D = XXX A, V_{DS} = XXX V V_{GS} = $V_{GS(off)}$ / $V_{GS(on)}$ R_{Gon} = X,XX Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	t_r				ns
Internal gate resistor	T_{vj} = 25°C		R_{Gint}		X,X		Ω

This formula ignores the internal resistance of the selected gate driver

Step 1:Calculation of IG and selection of gate driver IC

$$I_G = \frac{\Delta V_{GS,\text{datasheet}}}{R_{G,\text{datasheet}} + R_{G,\text{int}}}$$

$$\Delta V_{GS,\text{datasheet}} = |\, V_{GS(on)} \,| + |\, V_{GS(off)} \,|$$

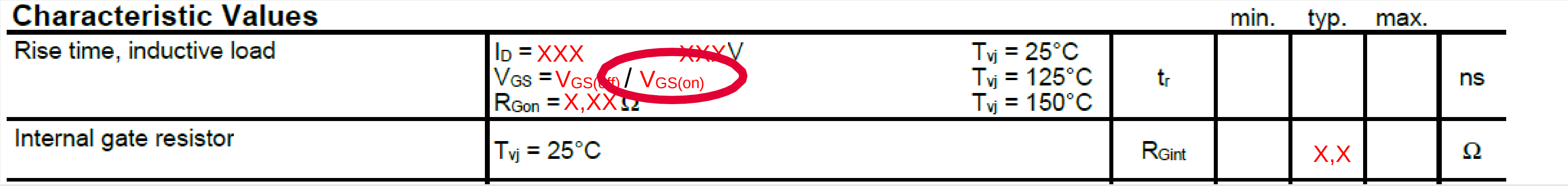


Characteristic Values				min.	typ.	max.	
Rise time, inductive load	I_D = XXX A, V_{DS} = XXX V V_{GS} = $V_{GS(off)}$ / $V_{GS(on)}$ R_{Gon} = X,XX Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	t_r				ns
Internal gate resistor	T_{vj} = 25°C		R_{Gint}		X,X		Ω

This formula ignores the internal resistance of the selected gate driver

Step 1:Calculation of IG and selection of gate driver IC

$$I_G = \frac{\Delta V_{GS,datasheet}}{R_{G,datasheet} + R_{G,int}} \Longrightarrow \Delta V_{GS,datasheet} = \underline{|\, V_{GS(on)} \,|} + |\, V_{GS(off)} \,|$$

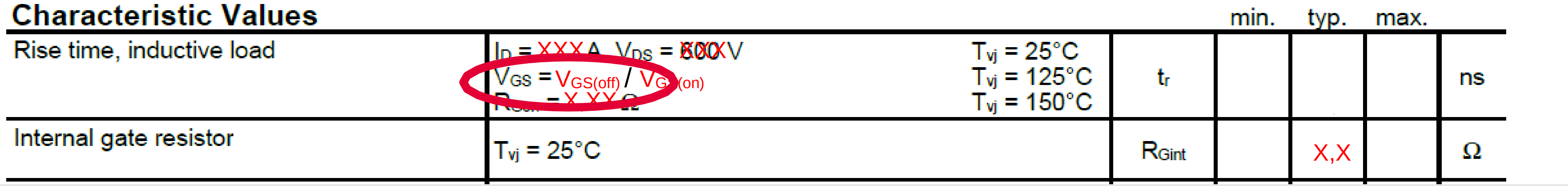


Characteristic Values				min.	typ.	max.	
Rise time, inductive load	I_D = XXX XXXV V_{GS} = $V_{GS(off)}$ / $V_{GS(on)}$ R_{Gon} = X,XX Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	t_r				ns
Internal gate resistor	T_{vj} = 25°C		R_{Gint}		X,X		Ω

This formula ignores the internal resistance of the selected gate driver

Step 1:Calculation of IG and selection of gate driver IC

$$I_G = \frac{\Delta V_{GS,\text{datasheet}}}{R_{G,\text{datasheet}} + R_{G,\text{int}}} \Longrightarrow \Delta V_{GS,\text{datasheet}} = |\,V_{GS(on)}\,| + \underline{|\,V_{GS(off)}\,|}$$

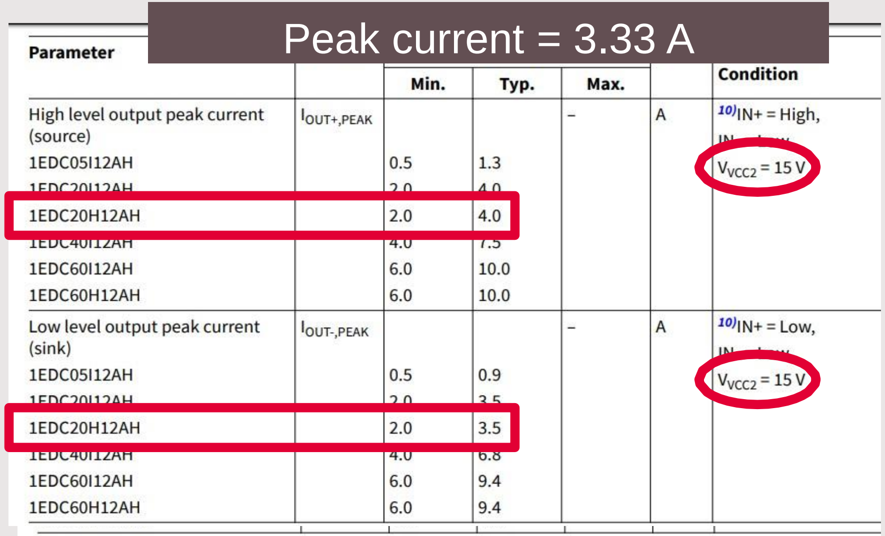


Characteristic Values				min.	typ.	max.	
Rise time, inductive load	I_D = XXX A, V_{DS} = XXX V V_{GS} = $V_{GS(off)}$ / $V_{GS(on)}$ R_{Gon} = X,XX Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	t_r				ns
Internal gate resistor	T_{vj} = 25°C		R_{Gint}		X,X		Ω

This formula ignores the internal resistance of the selected gate driver

Step 1:Calculation of IG and selection of gate driver IC

$$I_G = \frac{\Delta V_{GS,datasheet}}{R_{G,datasheet} + R_{G,int}}$$



Peak current = 3.33 A

Parameter		Min.	Typ.	Max.		Condition
High level output peak current (source)	$I_{OUT+,PEAK}$			–	A	[10] IN+ = High, IN– = Low, V_{VCC2} = 15 V
1EDC05I12AH		0.5	1.3			
1EDC20I12AH		2.0	4.0			
1EDC20H12AH		2.0	4.0			
1EDC40I12AH		4.0	7.5			
1EDC60I12AH		6.0	10.0			
1EDC60H12AH		6.0	10.0			
Low level output peak current (sink)	$I_{OUT-,PEAK}$			–	A	[10] IN+ = Low, IN– = Low, V_{VCC2} = 15 V
1EDC05I12AH		0.5	0.9			
1EDC20I12AH		2.0	3.5			
1EDC20H12AH		2.0	3.5			
1EDC40I12AH		4.0	6.8			
1EDC60I12AH		6.0	9.4			
1EDC60H12AH		6.0	9.4			

The selected gate driver should have a typical output current value equal or bigger than the calculated value

Step 2: Simple calculation for initial gate resistor

Peak gate current should be kept <u>**constant**</u> to allow the application to show the same switching and speeds provided in the datasheet

Step 2: Simple calculation for initial gate resistor

$$I_G = \frac{\Delta V_{GS,\mathrm{datasheet}}}{R_{G,\mathrm{datasheet}} + R_{G,\mathrm{int}}} = \frac{\Delta V_{GS,\mathrm{application}}}{R_{G,\mathrm{application}} + R_{G,\mathrm{int}}}$$

ΔV_{GS} depends on the application and usually has a fixed range of values

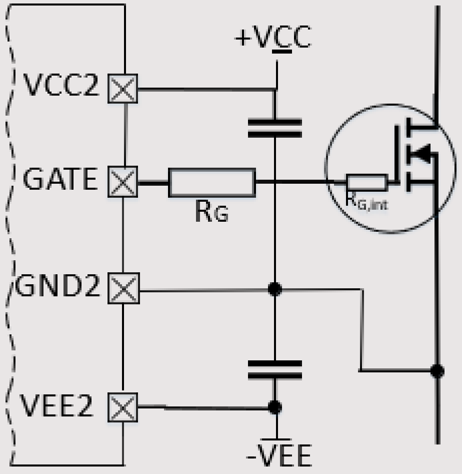
Step 2: Simple calculation for initial gate resistor

$$I_G = \frac{\Delta V_{GS,\text{datasheet}}}{R_{G,\text{datasheet}} + R_{G,\text{int}}} = \frac{\Delta V_{GS,\text{application}}}{R_{G,\text{application}} + R_{G,\text{int}}}$$

Easiest way to keep the peak gate current constant -adjust $R_{G,\text{application}}$

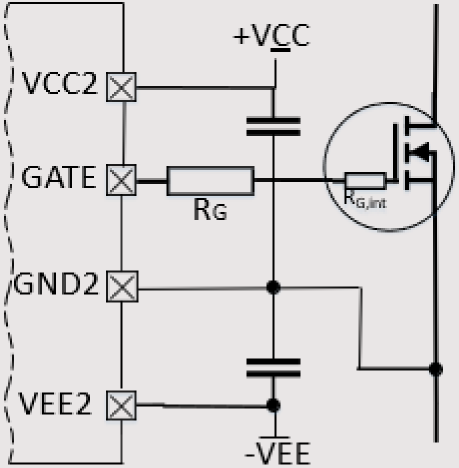
Step 2: Simple calculation for initial gate resistor

$$R_{G,application} = \frac{\Delta V_{GS,application}}{I_G} - R_{G,int} \Longrightarrow \Delta V_{GS,application} = |\underline{V_{VCC2}}| + |V_{VEE2}|$$



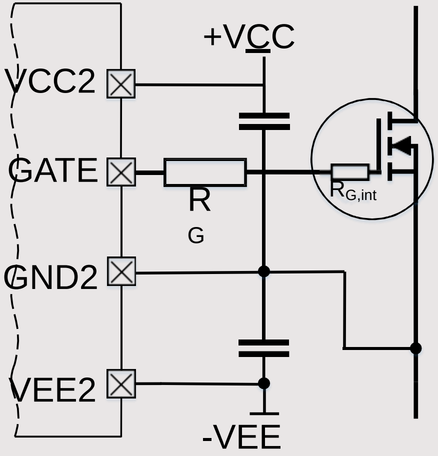
Step 2: Simple calculation for initial gate resistor

$$R_{G,application} = \frac{\Delta V_{GS,application}}{I_G} - R_{G,int} \Rightarrow \Delta V_{GS,application} = |\, V_{VCC2} \,| + |\, \underline{V_{VEE2}} \,|$$



Step 2: Simple calculation for initial gate resistor

$$R_{G,application} = \frac{\Delta V_{GS,application}}{I_G} - R_{G,int} \Longrightarrow \Delta V_{GS,application} = |V_{VCC2}| + |V_{VEE2}|$$



It is recommended to use **negative gate voltage for SiC MOSFETs**
to ensure that the device stays turned off during the operation of the power converter

Step 3:Simplified calculation of the power dissipation for the gate driver

$$P_D = Q_{G,application} \cdot f_{sw} \cdot \Delta V_{GS,application}$$

Calculations are simplified assuming that the power losses during switching are only dissipated in the output stage of the gate driver

Step 3:Simplified calculation of the power dissipation for the gate driver

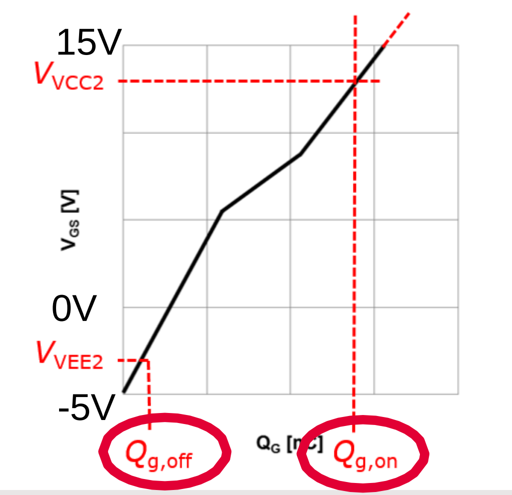
$$P_D = Q_{G,\text{application}} \cdot f_{sw} \cdot \Delta V_{GS,\text{application}}$$

In reality: Gate resistances also take over some of the losses!

Calculations are simplified assuming that the power losses during switching are only dissipated in the output stage of the gate driver

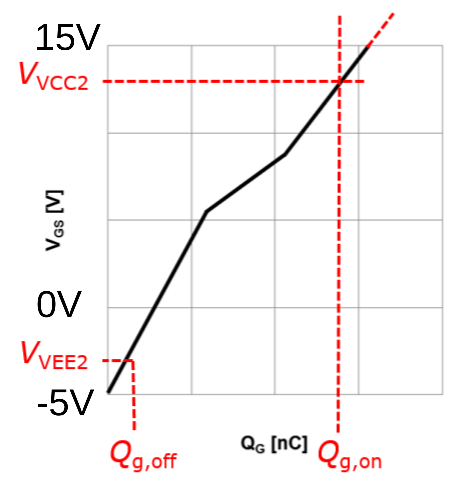
Step 3:Simplified calculation of the power dissipation for the gate driver

$$P_D = \underline{\underline{Q_{G,application}}} \cdot f_{sw} \cdot \Delta V_{GS,application}$$



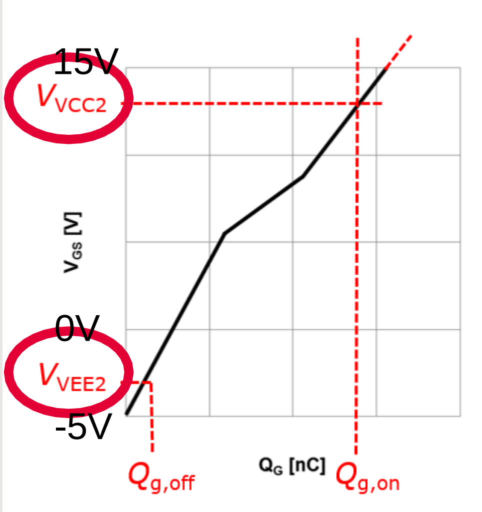
Step 3:Simplified calculation of the power dissipation for the gate driver

$$P_D = Q_{G,application} \cdot \underline{\underline{f_{sw}}} \cdot \Delta V_{GS,application}$$



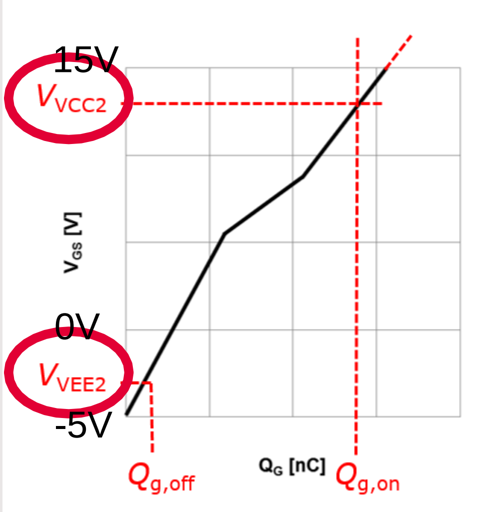
Step 3:Simplified calculation of the power dissipation for the gate driver

$$P_D = Q_{G,application} \cdot f_{sw} \cdot \underline{\underline{\Delta V_{GS,application}}}$$



Step 3:Simplified calculation of the power dissipation for the gate driver

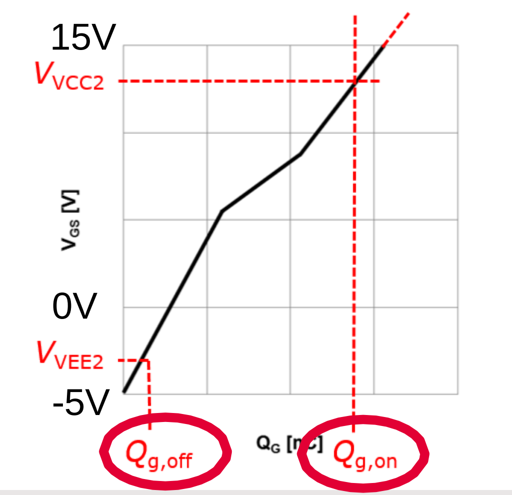
$$P_D = Q_{G,\text{application}} \cdot f_{sw} \cdot \Delta V_{GS,\text{application}}$$



Step 3:Simplified calculation of the power dissipation for the gate driver

$$P_D = \underline{Q_{G,application}} \cdot f_{sw} \cdot \Delta V_{GS,application}$$

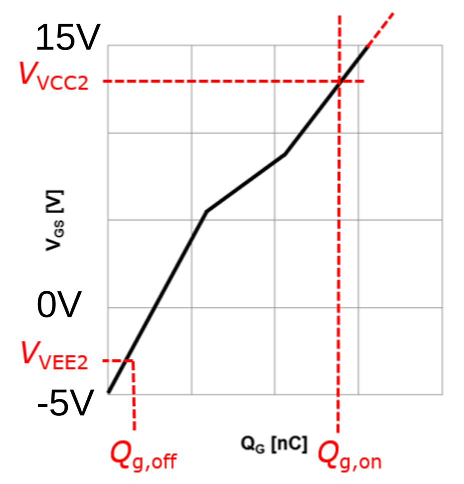
$$Q_{G,application} = Q_{g,on} - Q_{g,off}$$



Gate charge of the application can be calculated as the difference between on-state gate charge and off-state gate charge

Step 3:Simplified calculation of the power dissipation for the gate driver

$$P_D = Q_{G,\text{application}} \cdot f_{sw} \cdot \Delta V_{GS,\text{application}}$$



We can **calculate the power dissipated** in the gate driver circuit
knowing the **target switching application** and the **supply voltage** for the gate driver

Step 3:Simplified calculation of the power dissipation for the gate driver

$$P_D = Q_{G,application} \cdot f_{sw} \cdot \Delta V_{GS,application} \leq P_{D,OUT,datasheet}$$

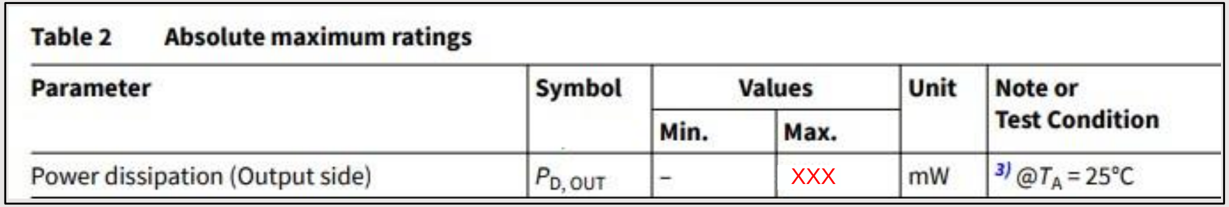
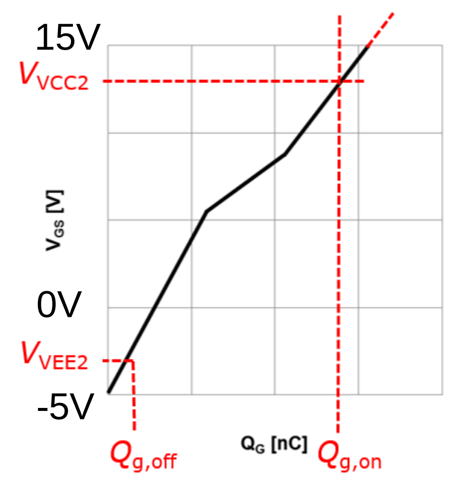


Table 2 Absolute maximum ratings

Parameter	**Symbol**	**Values**		**Unit**	**Note or Test Condition**
		Min.	**Max.**		
Power dissipation (Output side)	$P_{D,OUT}$	–	XXX	mW	3) @$T_A = 25°C$



Linear derating of the power dissipation has to be considered between:

$P_{D,OUT}$ test condition point + maximum junction temperature

Step 3:Simplified calculation of the power dissipation for the gate driver

$$P_D = Q_{G,application} \cdot f_{sw} \cdot \Delta V_{GS,application} \quad \leq \underline{P_{D,OUT,datasheet}}$$

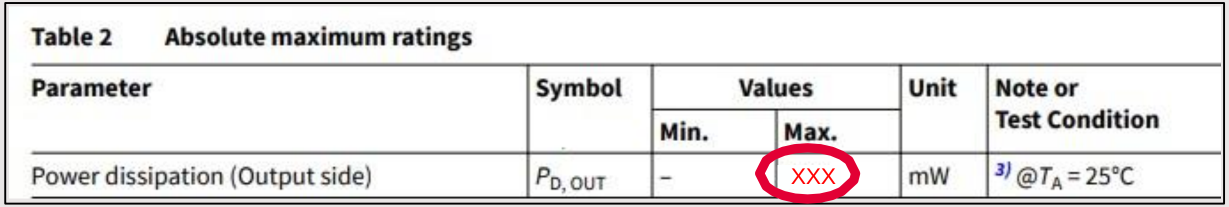
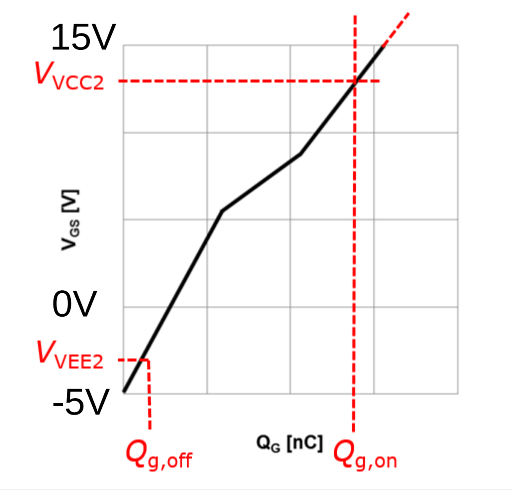


Table 2 Absolute maximum ratings

Parameter	**Symbol**	**Values**		**Unit**	**Note or Test Condition**
		Min.	**Max.**		
Power dissipation (Output side)	$P_{D,OUT}$	–	XXX	mW	[3] @T_A = 25°C

Result ≤ absolute maximum power dissipation $P_{D,OUT}$ in output side of gate driver



Linear derating of the power dissipation has to be considered between:

$P_{D,OUT}$ test condition point + maximum junction temperature

Step 4 :Target of laboratory verification

Gate driver circuit

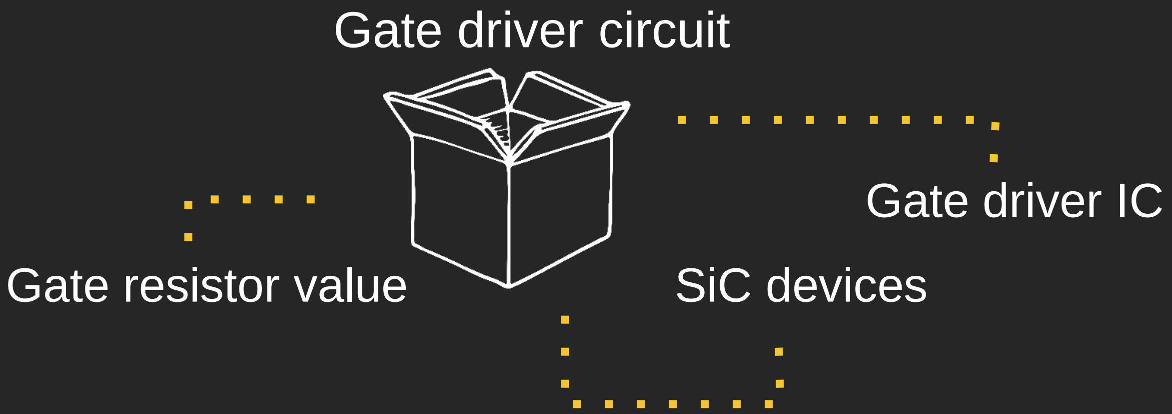
Gate driver IC

Gate resistor value

SiC devices

Components were selected -design verification in laboratory is required

Step 4 :Target of laboratory verification



Lab measurements prove that assumptions and calculations result in safe switching of SiC transistor

Step 4 :Target of laboratory verification

3 basic tests
are recommended

Validations to prove the absence of **parasitic turn-on** triggered by dv/dt under worst case conditions

Worst-case conditions are operations
under lowest application temperatures, lowest drain current and worst-case gate-source voltage

Step 4 :Target of laboratory verification

3 basic tests
are recommended

Validations to prove the absence of **parasitic turn-on** triggered by dv/dt under worst case conditions

Measurement of
gate driver IC temperature
during steady state operation

It is easier to use an **IR camera -thermocouples** can also be useful

Step 4 :Target of laboratory verification

3 basic tests are recommended

Validations to prove the absence of **parasitic turn-on** triggered by dv/dt under worst case conditions

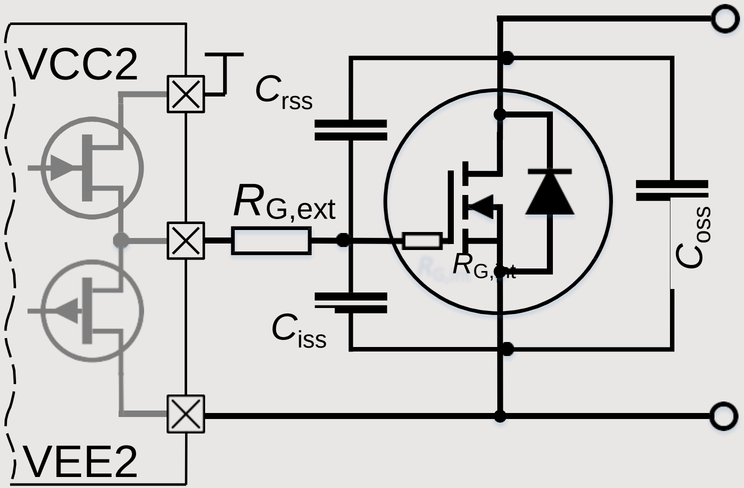
Validation of **gate resistor's loading** (R_G)

Measurement of **gate driver IC temperature** during steady state operation

IR camera can help getting the heating of elements Peak power of the resistor - calculated and checked against the single pulse rating of the resistor

Step 4 :First test Parasitic turn-on robustness

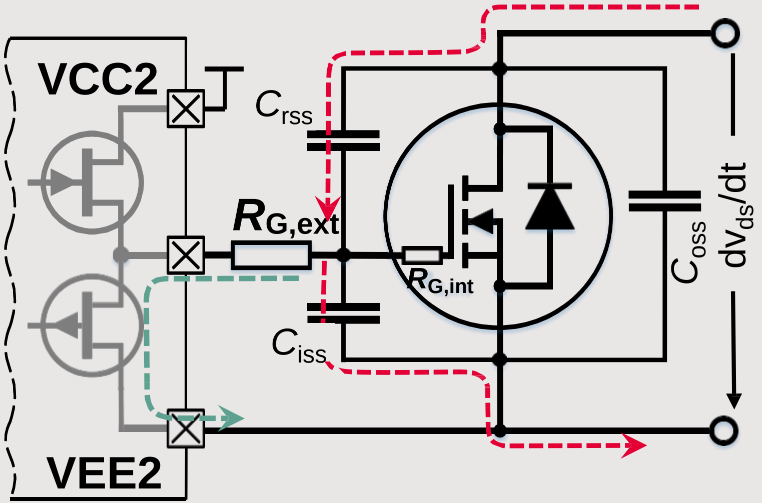
Gate driving circuit w/ a SiC power device + gate driver output stage + external gate resistor



Parasitic capacitances are always **present** and **should not be ignored**!

Step 4 :First test Parasitic turn-on robustness

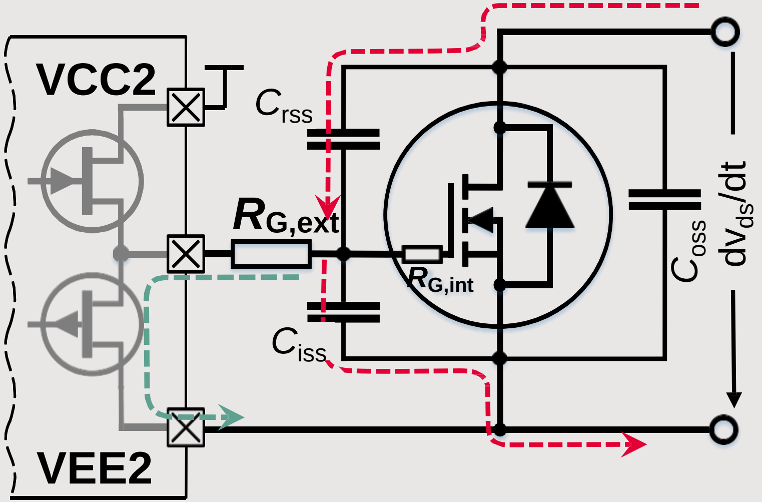
Gate driving circuit w/ a SiC power device + gate driver output stage + external gate resistor



Capacitive voltage divider □ increase voltage at gate terminal

Step 4 :First test Parasitic turn-on robustness

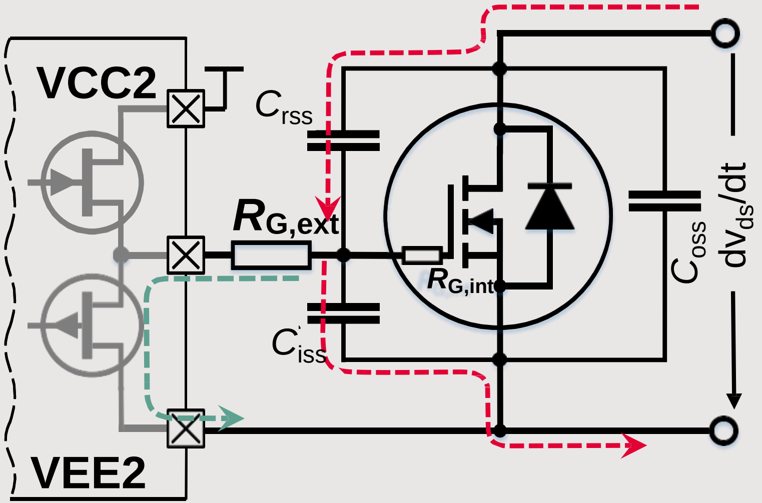
Gate driving circuit w/ a SiC power device + gate driver output stage + external gate resistor



If voltage at gate ≥ gate threshold voltage $V_{GS(th)}$ -transistor could turn on

Step 4 :First test Parasitic turn-on robustness

Gate driving circuit w/ a SiC power device + gate driver output stage + external gate resistor



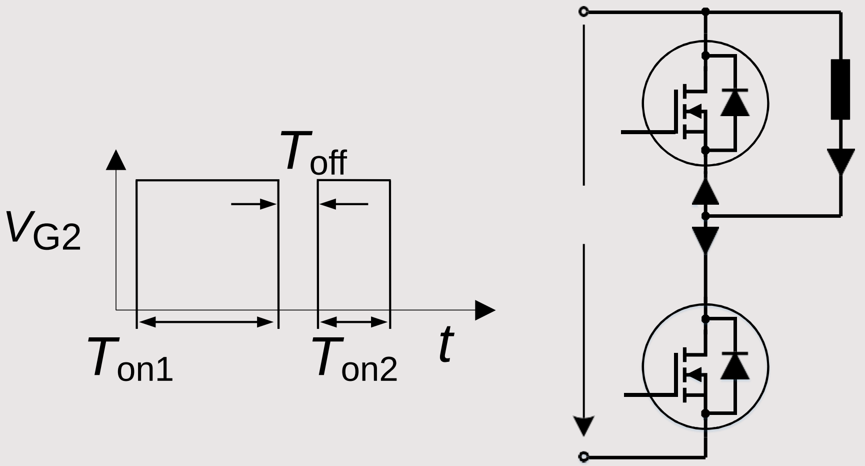
Gate resistor should be adjusted to mitigate this:
through the **design of a different gate resistor** or by using an **active miller clamp**

Step 4 :First test Parasitic turn-on robustness

Parasitic turn-on should never occur

Use double pulse test

- High/Low drain current $I_D = 0\ A / I_{nom}$
- High/Low temperature $T_j = $ Min. / Max
- Nominal gate voltages
- Test both sides of the half-bridge



Step 4 :First test Parasitic turn-on robustness

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- High/Low temperature T_j = Min. / Max
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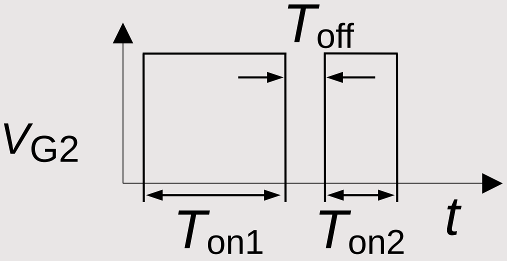
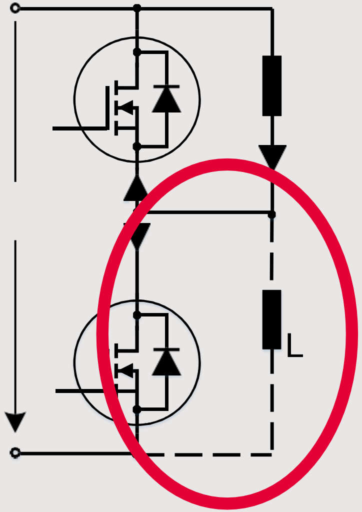
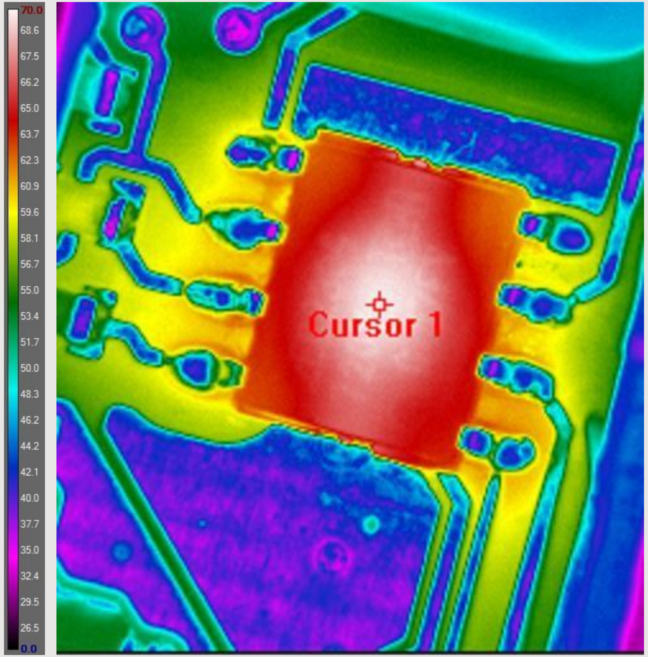




Step 4 : Second test Temperature investigation of IC using IR camera

During thermal steady state operation,
case temperature can be recorded



Ideally tested under expected operating ambient temperature!

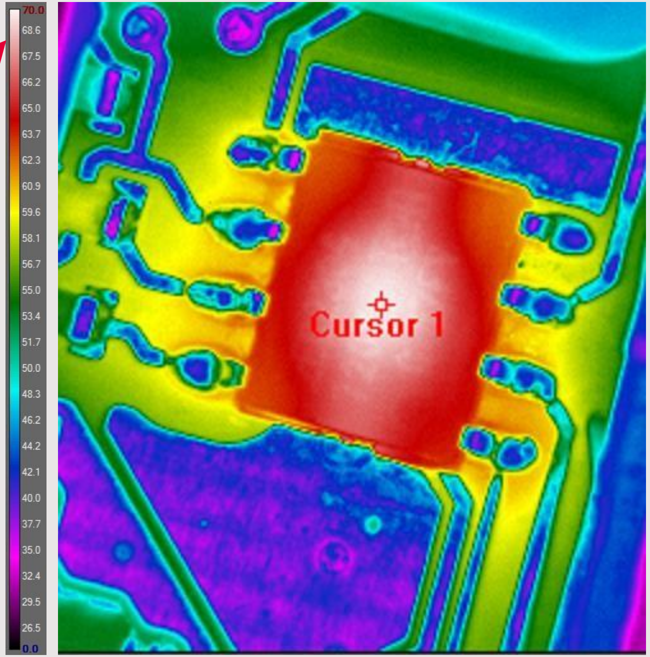
Step 4 : Second test Temperature investigation of IC using IR camera

During thermal steady state operation,
case temperature can be recorded

Record case temperature with a thermal camera

Junction temperature can be calculated

$$T_J = P_D \cdot \Psi_{\mathrm{th,jt}} + \underline{\mathrm{T}_{\mathrm{case}}}$$



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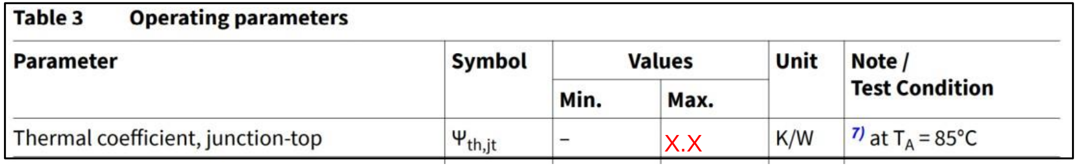
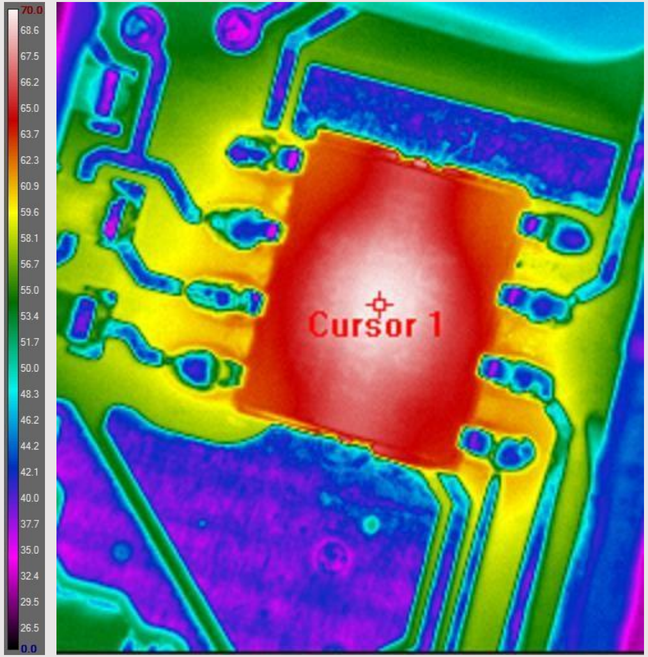


Table 3 Operating parameters

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Thermal coefficient, junction-top	$\Psi_{th,jt}$	–	X.X	K/W	7) at T_A = 85°C



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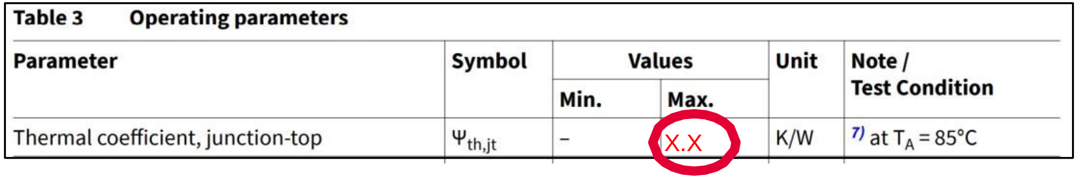
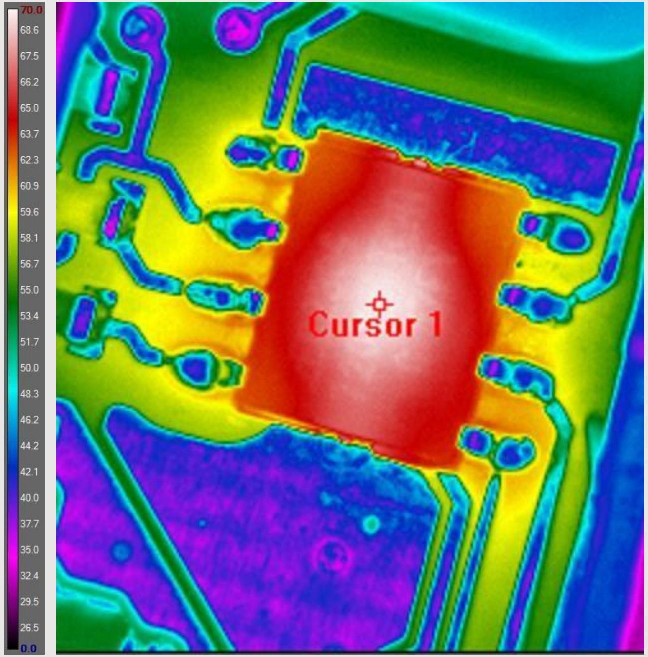


Table 3 Operating parameters

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Thermal coefficient, junction-top	$\Psi_{th,jt}$	–	X.X	K/W	7) at $T_A = 85°C$



Step 4 : Second test Temperature investigation of IC using IR camera

During thermal steady state operation,
case temperature can be recorded

Record case temperature with a thermal camera

Junction temperature can be calculated

$$T_J \leq \underline{T_{J\,,\max}}$$

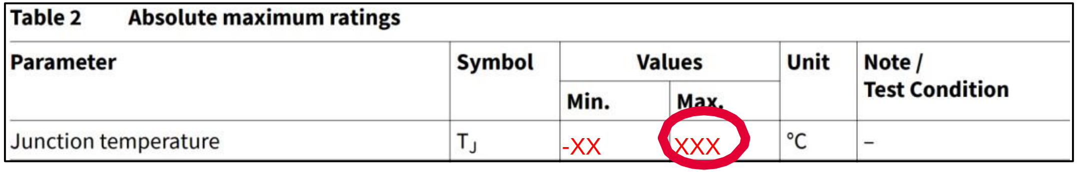
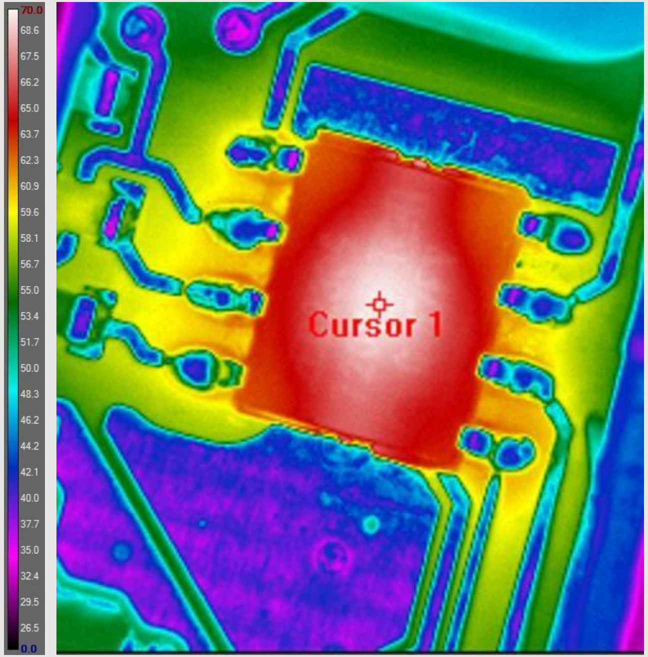


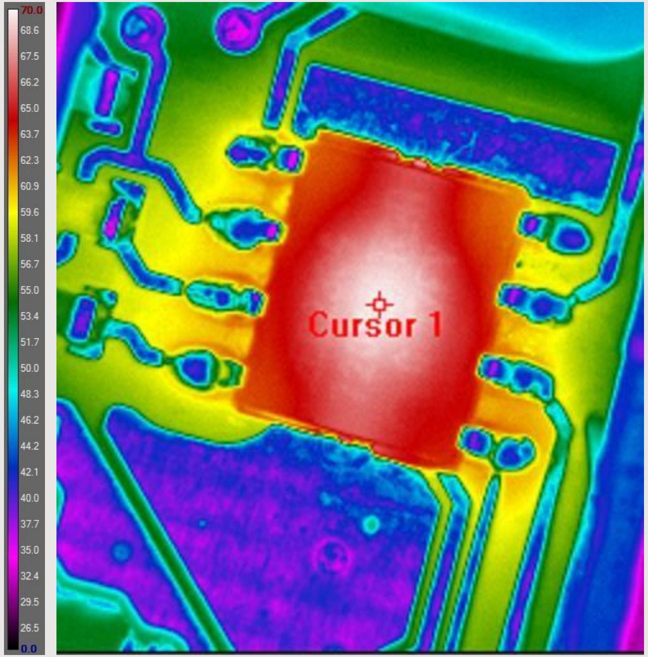
Table 2 **Absolute maximum ratings**

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Junction temperature	T_J	-XX	XXX	°C	–



Step 4 : Third test Calculation of peak power stress in gate resistors

During steady state operation, ***R***



A good way to measure R_G temperature (especially if IR camera is used) is during case temperature measurement for the gate driver IC

Summary

Gate drivers design has to support SiC MOSFET's characteristics

SiC MOSFET's switching behavior has to be verified experimentally

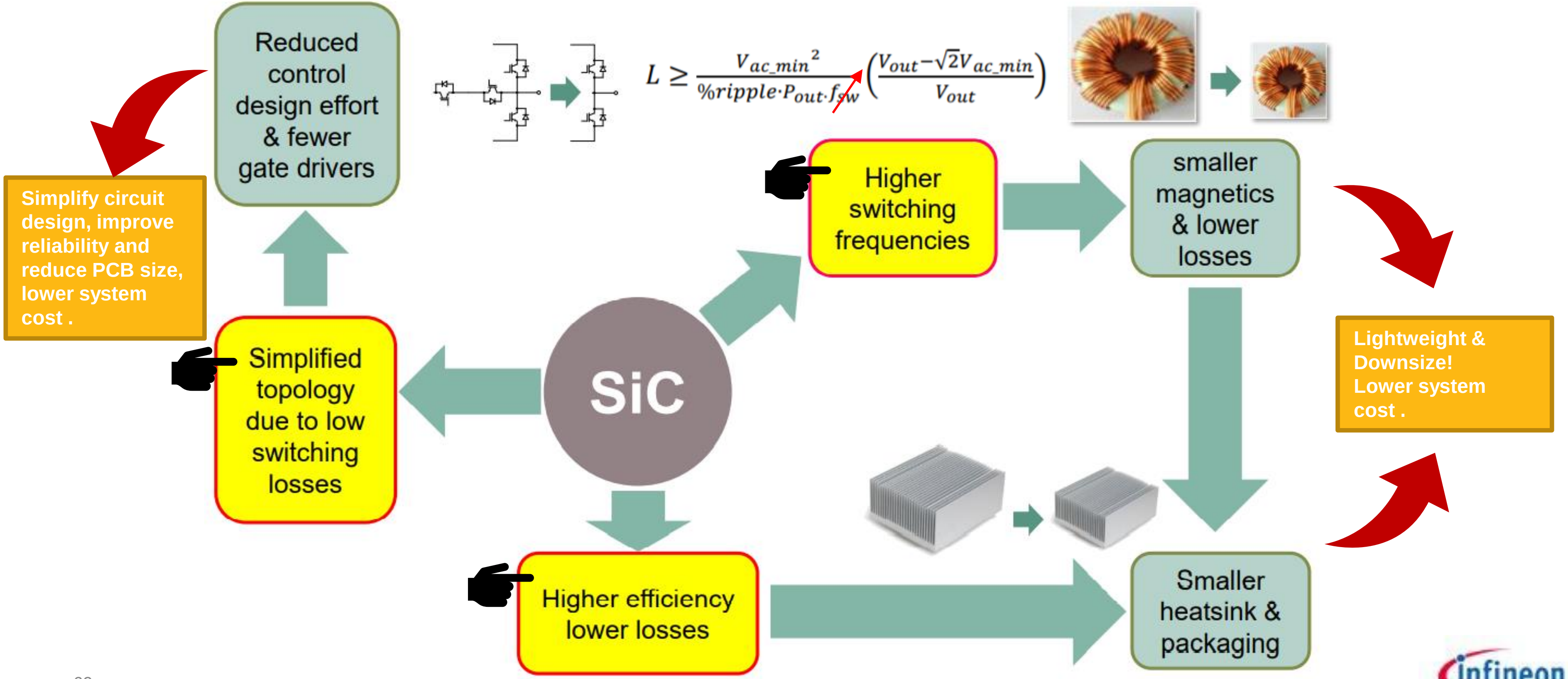
Power dissipation of the gate driver circuit has to be verified by calculation and temperature measurements

Recommended EiceDRIVER™ for SiC MOSFETs

Product	Part Number	Typ. Peak Drive Current	VCC2-VEE2	Typ.UVLO Thresholds	Typ. Prop. Delay	Miller Clamp	Other Key Features	Package
1EDI Compact Isolated High-Side Driver Family	1EDI20N12AF	3.5 A	35 V	9.1 V / 8.5 V	≤ 120 ns	No	Functional Isolation	DSO-8 150 mil 
	1EDI60N12AF	9.4 A	35 V	9.1 V / 8.5 V	≤ 120 ns	No		
	1EDI20I12MF	3.5 A	20 V	11.9 V / 11 V	≤ 300 ns	Yes		
	1EDI20H12AH	3.5 A	35 V	12 V / 11.1 V	≤ 125 ns	No	8 mm Creepage Clearance **UL V_{RMS} 3 kV certified** versions will be available in July 2017	DSO-8 300 mil 
	1EDI60H12AH	9.4 A	35 V	12 V / 11.1 V	≤ 125 ns	No		
	1EDI20I12MH	3.5 A	20 V	11.9 V / 11 V	≤ 300 ns	Yes		
1ED-F2 Isolated High-Side Driver with Integrated Protection	1ED020I12-F2	2.0 A	28 V	12 V / 11 V	≤ 170 ns	Yes	Short circuit clamping; DESAT protection; Active shutdown	DSO-16 
2ED-F2 Isolated Dual High-Side Driver with Integrated Protection	2ED020I12-F2	2.0 A	28 V	12 V / 11 V	≤ 170 ns	Yes		DSO-36 
1EDS Slew Rate Control (SRC) Isolated High- Side Driver	1EDS20I12SV	2.0 A	28 V	11.9 V / 11 V	≤ 485 ns	Yes	Real-time adjustable gate current control; Over-current protection, Soft turn-off shut down, Two-level turn-off	DSO-36 

Success Stories

Benefits that SiC MOSFET bring to system



Reduced control design effort & fewer gate drivers

Simplify circuit design, improve reliability and reduce PCB size, lower system cost .

$$L \geq \frac{V_{ac\_min}^{2}}{\%ripple \cdot P_{out} \cdot f_{sw}} \left(\frac{V_{out}-\sqrt{2}V_{ac\_min}}{V_{out}}\right)$$

Higher switching frequencies

smaller magnetics & lower losses

Lightweight & Downsize! Lower system cost .

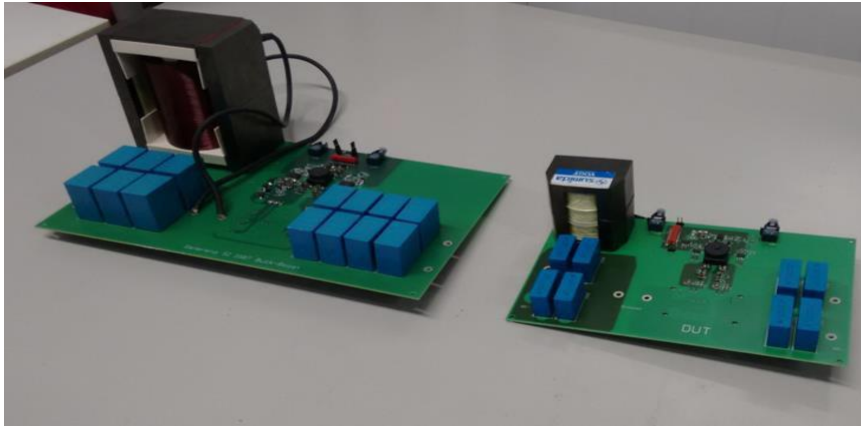
Simplified topology due to low switching losses

SiC

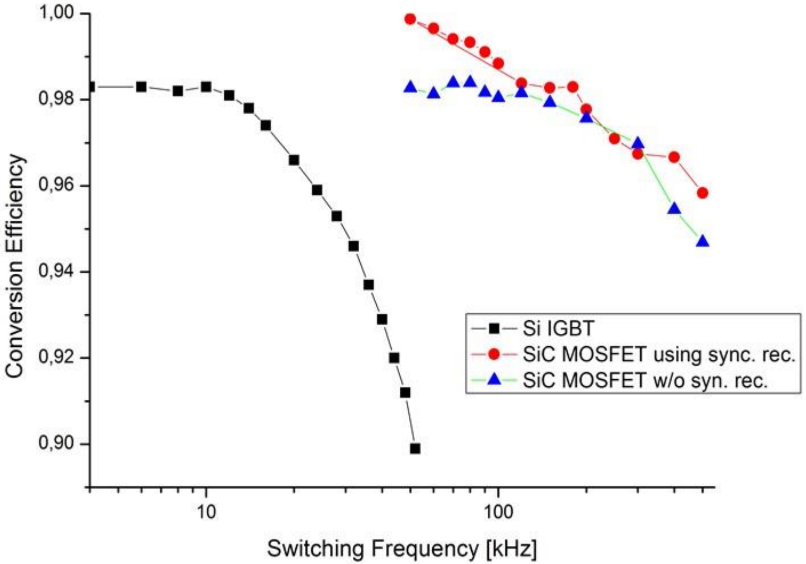
Higher efficiency lower losses

Smaller heatsink & packaging

Benefits that SiC MOSFET bring to system



		SI IGBT Reference	SiC MOSFET Demonstrator
L	Size (H x W x L) [mm^3]	125 x 95 x 70	70 x 55 x 40
	Weight	3.20 kg	0.50 kg
Total	Size (H x W x L) [mm^3]	139 x 300 x 185	84 x 206 x 134
	Weight	3.77 kg	0.93 kg



SiC MOSFET vs Si IGBT

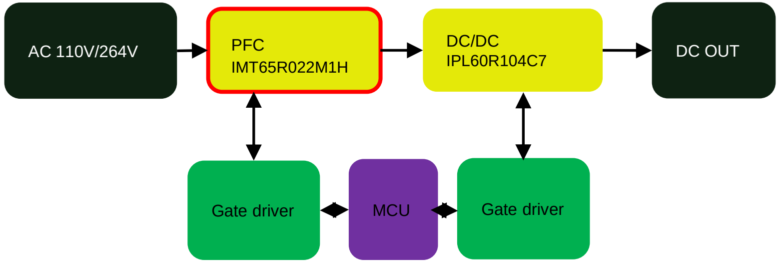
Successful stories

1

Power Supplies

Successful case: Brick Power

Block Diagram



AC 110V/264V

PFC
IMT65R022M1H

DC/DC
IPL60R104C7

DC OUT

Gate driver

MCU

Gate driver

Application

- Project: 750 half brick power

Benefit

- High power density

(From Brick power to half brick- Volume 50% reduction)

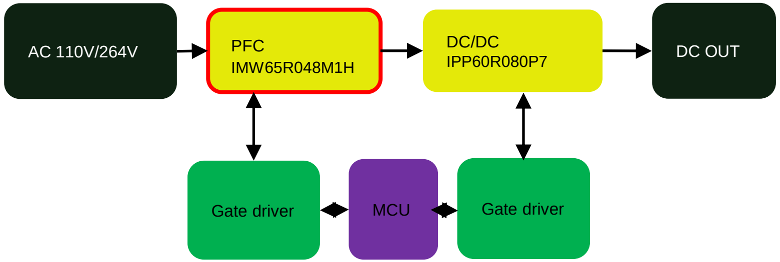
- Increase efficiency
- Provide better temperature performance

Key Component

SiC MOSFET:
IMT65R022M1H 1pcs/set

Successful case: 1200W server power

Block Diagram



Application

- Project: 1200W Server power

Benefit

- High power density(Volume 1/3 reduction)
- Increase efficiency
- Provide better temperature performance

Higher reliability at high temperatures and lower power loss.

Key Component

SIC MOSFET:
IMW65R048M1H 1pcs/set

Successful case: 25KW X-ray Power

Block Diagram


AC 220/380V
Full Bridge
FF8MR12W2M1
High voltage transformer
Voltage Doubler
X-Ray Light

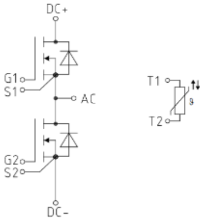
Application

- Project: 25KW X-ray Power

Benefit

- High power density
- Increase efficiency
- Provide better temperature performance

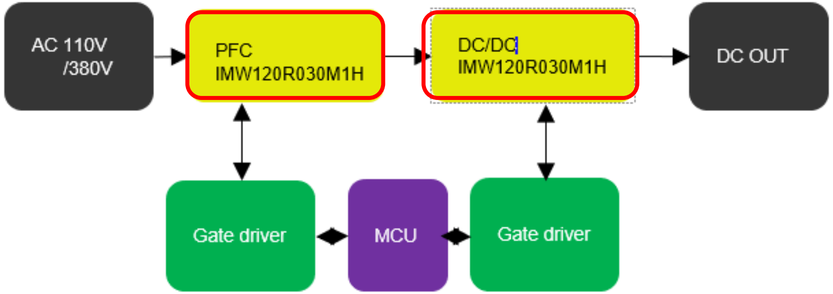
Key Component



SIC Module:
FF8MR12W2M1_B11 2pcs/set

Successful case: Bidirectional DC Power Supply

Block Diagram



Application

- Project: 18kW DC source

Benefit

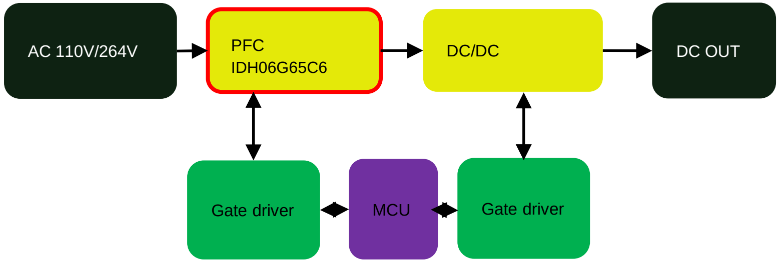
- High power density
- Increase efficiency
- Provide better temperature performance

Key Component

SIC MOSFET:
IMW120R030M1H 2pcs/set

Successful case: 450W AC-DC Power for Telecom

Block Diagram



AC 110V/264V

PFC
IDH06G65C6

DC/DC

DC OUT

Gate driver

MCU

Gate driver

Application

- Project: 450W AC-DC POWER FOR TELECOM

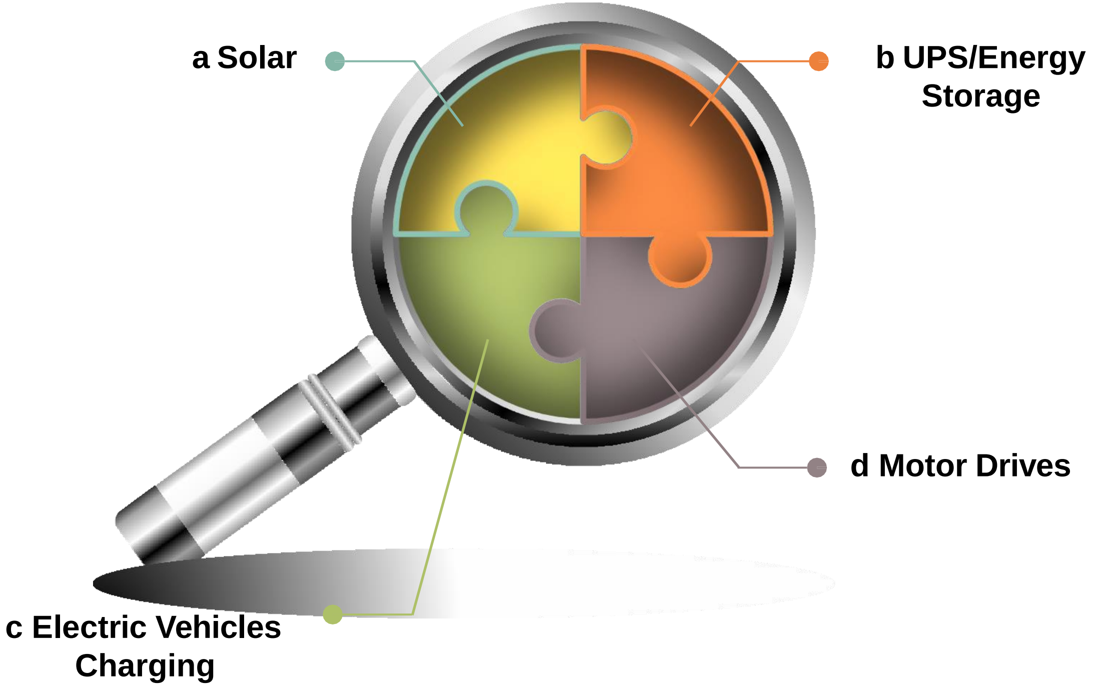
Benefit

- High power density
- Increase efficiency
- Provide better temperature performance

Key Component

SIC DOODE:
IDH06G65C6 1pcs/set

Some Different Possible Application Areas for SiC



a Solar

b UPS/Energy Storage

c Electric Vehicles Charging

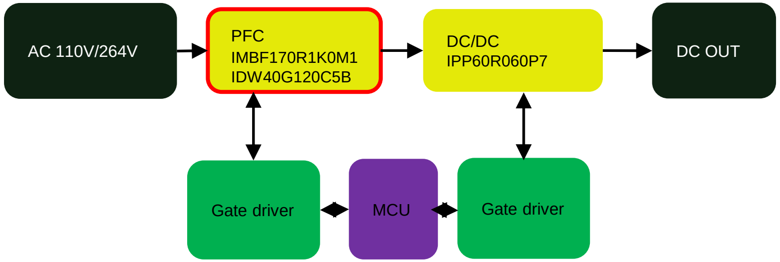
d Motor Drives

Successful stories

② UPS &
Energy Storage System

Successful case: 20KW UPS System

Block Diagram



AC 110V/264V

PFC
IMBF170R1K0M1
IDW40G120C5B

DC/DC
IPP60R060P7

DC OUT

Gate driver

MCU

Gate driver

Application

- Project: 20KW UPS System

Benefit

- High power density
- Increase efficiency
- Provide better temperature performance

Meet IDC(Internet Data Center)Requirements, Higher reliability at high temperatures and lower power loss.

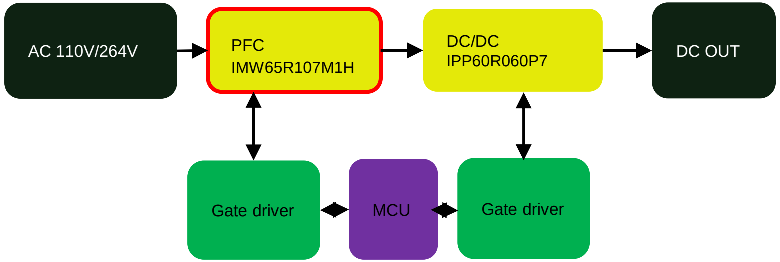
Key Component

SiC MOSFET: IMBF170R1K0M1 1pcs/Set

SiC Diode:IDW40G120C5B 1pcs/Set

Successful case: Off-line UPS

Block Diagram



Application

- Project: Backup power source (AC/DC power)

Benefit

- High power density (Lightweight, downsize)
- Increased efficiency
- Provide better temperature performance

Key Component

SiC Diode: IDH06G65C5

Energy Storage System with SiC

Development of Kaco inverter

Year 2008, 100 kW, 1129 kg, 2,12m Height

Si

Year 2011, 50 kW, 151 kg 1,36 m Height

Si

Year 2016, 50 kW, 70 kg, 0,76 m Height

Si

Year 2018, 125 kW, 77 kg, 0,72 m Height

SiC

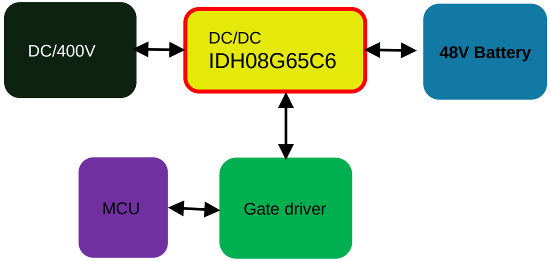
Value proposition

- Power density increase by factor 2.5 (50kW - 125kW)
- Reduction of number of switches (5-level to 3-level), reduce risk of failed failures
- Use of SiC enable higher efficiency at high operation temperature
- Source: https://www.pv-magazine.de/2018/11/14/pv-magazine-top-innovation-kacos-neuer-siliziumkarbid-wechselrichter/

Power density increases by 2.5x

Successful case: 3.3KW Energy Storage System

Block Diagram



Application

- Project: 3.3KW Energy storage system for factory

Benefit

- Higher power density
- Higher efficiency
- Smaller size and weight of systems
- Robustness and higher system reliability

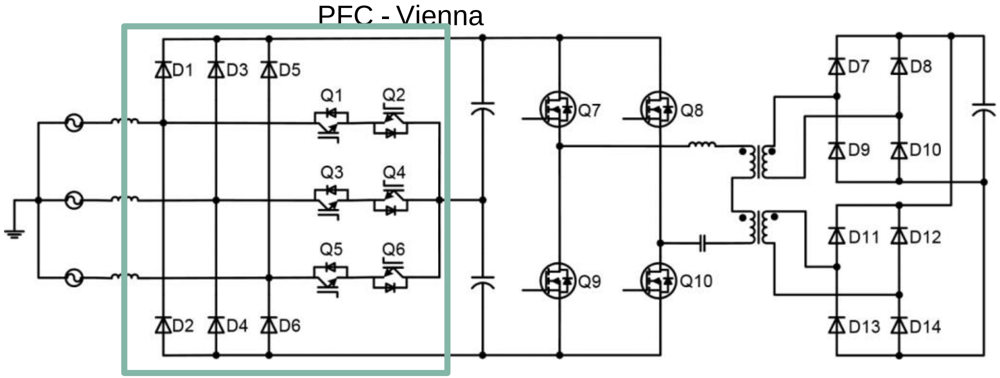
Key Component

SiC DIODE:
IDH08G65C6 2pcs/set

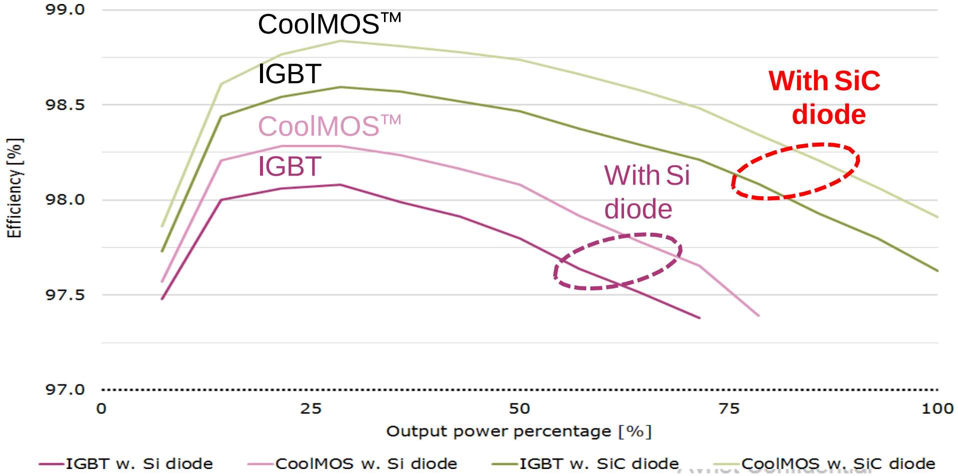
Successful stories

④ Electric Vehicle (EV) Charging

EV charger PFC stage



SiC diode is the key for high efficiency and high output power.



SiC vs. Si diode:

- +0.8% higher efficiency

for >80% increased output power!

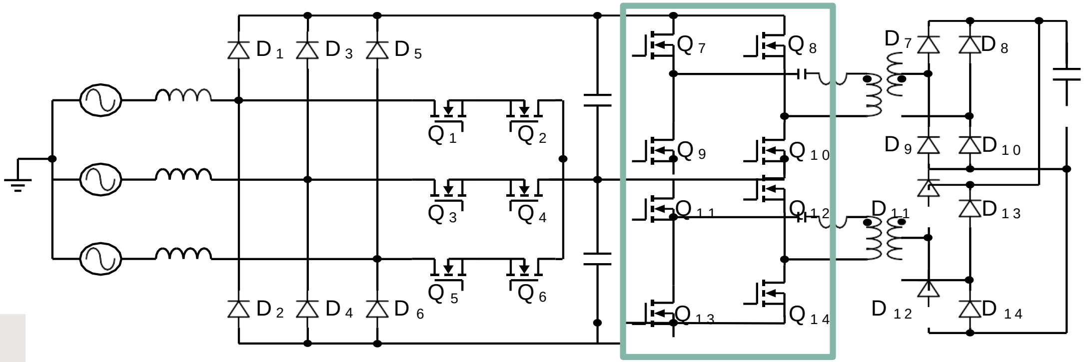
EV charger DC-DC stage

1200V SiC MOSFET to simplify system with high power density.

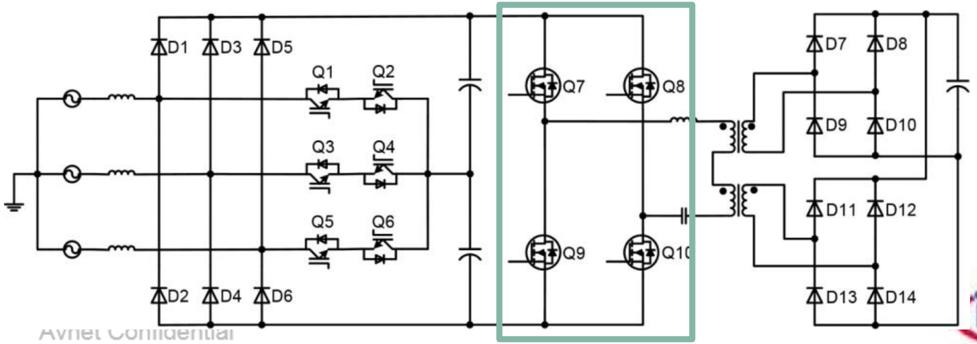
Si to SiC solution in DC/DC:

- 2x Full Bridge to 1x Full Bridge
- Reduced part count
- Less number of semiconductor parts on the current path
- Potential smaller size magnetics

DC/DC- 2x Full Bridge LLC with 600V MOSFET

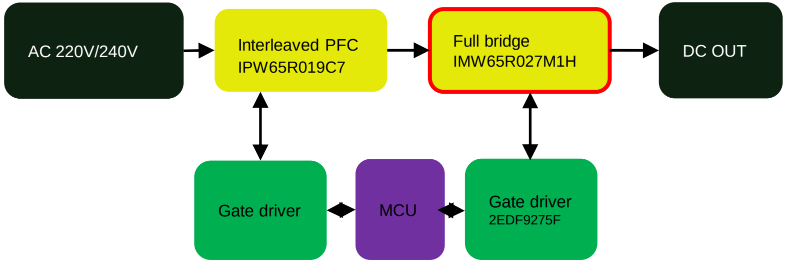


DC/DC- 1x Full Bridge LLC with 1200V CoolSiC



Successful case: 12KW Charging Pile

Block Diagram



AC 220V/240V

Interleaved PFC
IPW65R019C7

Full bridge
IMW65R027M1H

DC OUT

Gate driver

MCU

Gate driver
2EDF9275F

Application

- Project: 12KW Charging pile

Benefit

- Increased efficiency
- Fast charging cycles
- High power density

Minimize the size and weight of the charging station-Easy to install

Key Component

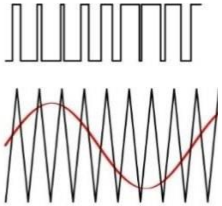
infineon

SiC MOSFET:
IMW65R027M1H 4pcs/set

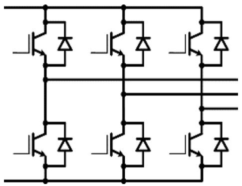
Successful stories

4 Motor drive

No magnetics

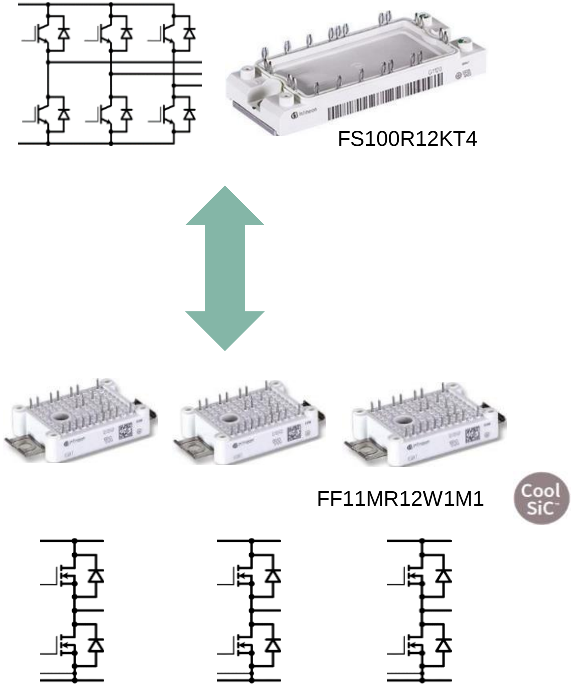


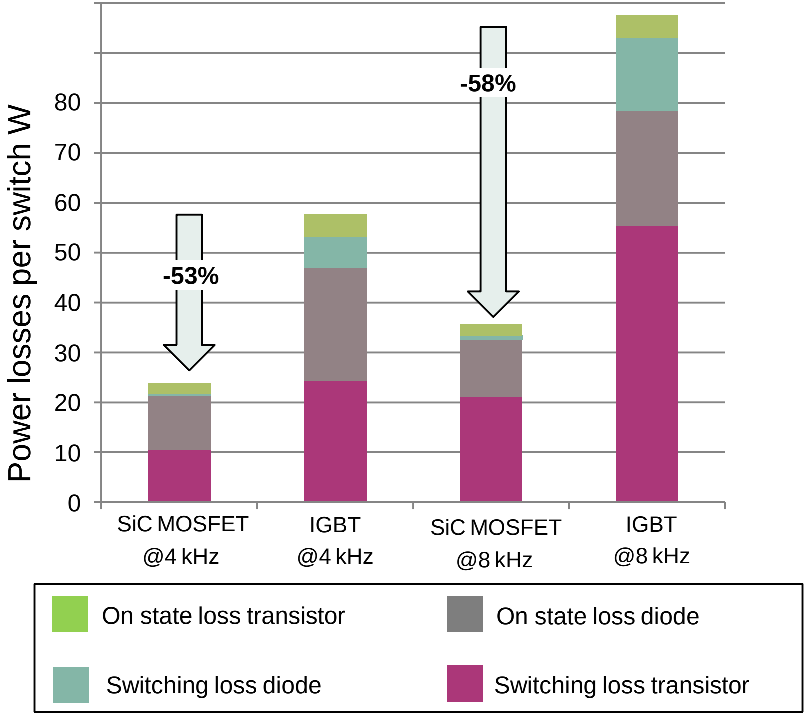
Typical ≈ 4 kHz



Simple topology

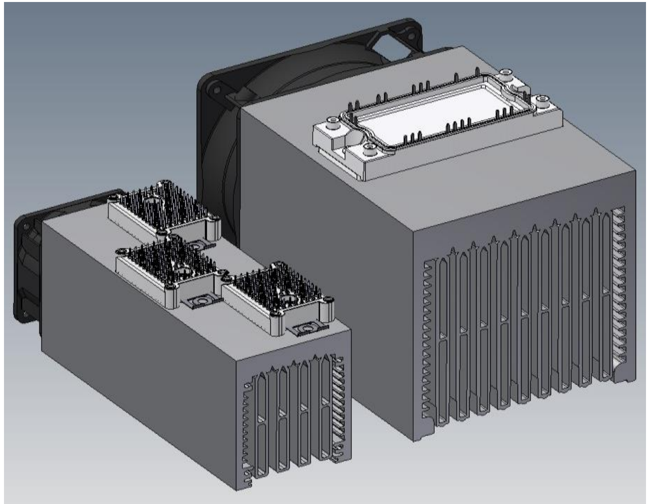
SiC and Si for a 22 kW 480V$_{AC}$





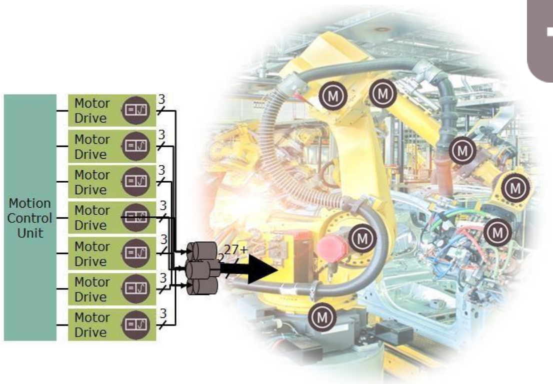
Lower losses bring lower weight, size and cooling effort

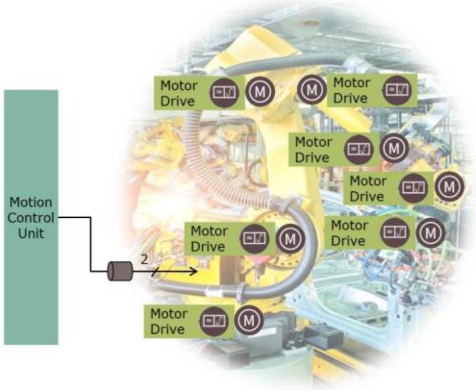
Drives



60% size and weight reduction

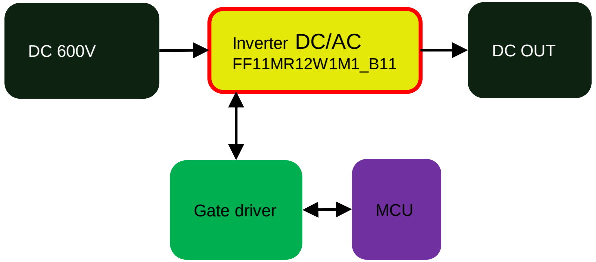
For some applications, weight & size are key design parameters.





Successful case: 15KW motor drive for Fuel Cell Bus Air Compressor

Block Diagram



DC 600V

Inverter DC/AC
FF11MR12W1M1_B11

DC OUT

Gate driver

MCU

Application

- Project: 15KW motor drive for fuel cell bus air compressor

Benefit

- SiC can reduce switching loss, suitable for 45KHz applications and high power 15KW application

(Reduce noise and increase control stability)

- Increased efficiency
- Higher power density (Lightweight, downsize)

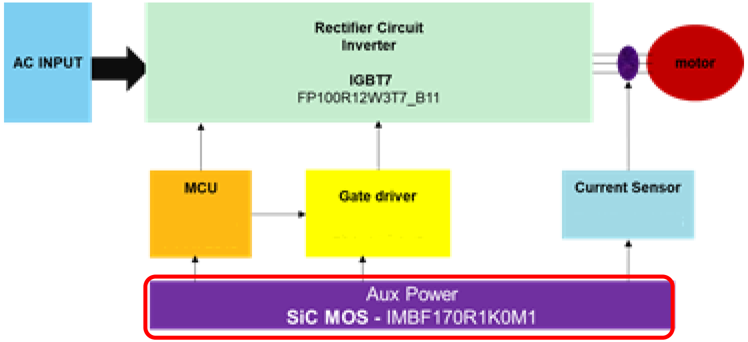
Key Component

infineon

SiC MOSFET Modules:
FF11MR12W1M1_B11 3pcs/Set

Successful case: 22kW Industrial Drive

Block Diagram



Application

- Project: Industrial Drive 22kW

Benefit

- Reduce the size of the auxiliary power transformer and heatsink
- Increased efficiency
- High power density

(Reduce the size and weight of the drive)

Key Component

SiC MOSFET:
IMBF170R1K0M1 1pcs/set

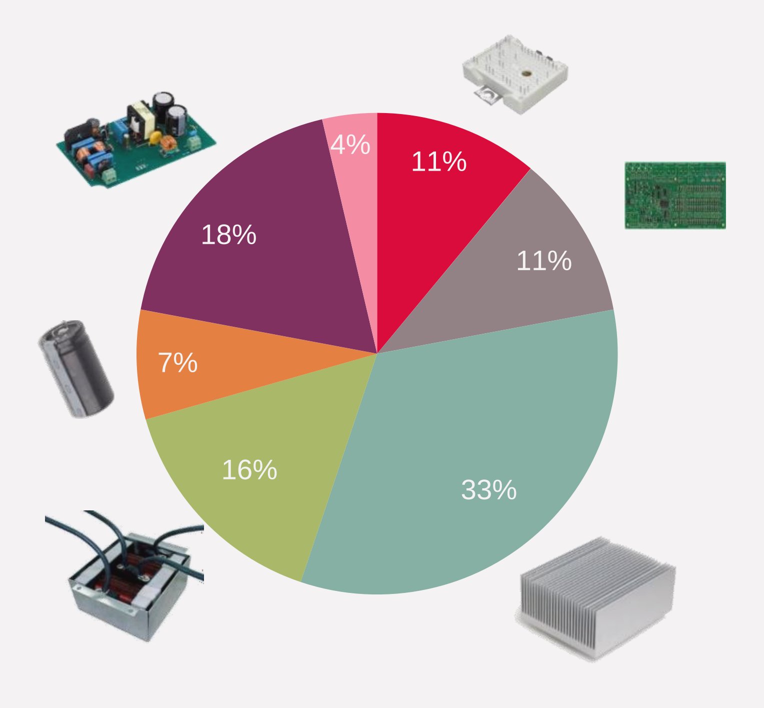
Typical appearance

Successful stories

5 Solar Applications

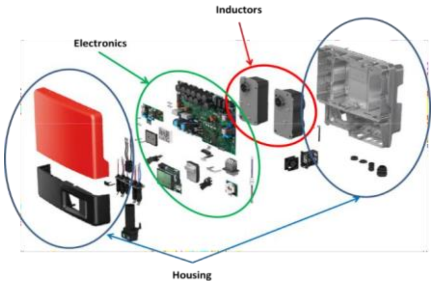
Solar Applications: Why is SiC a Good Fit?

Example - PV String Inverter BOM Cost



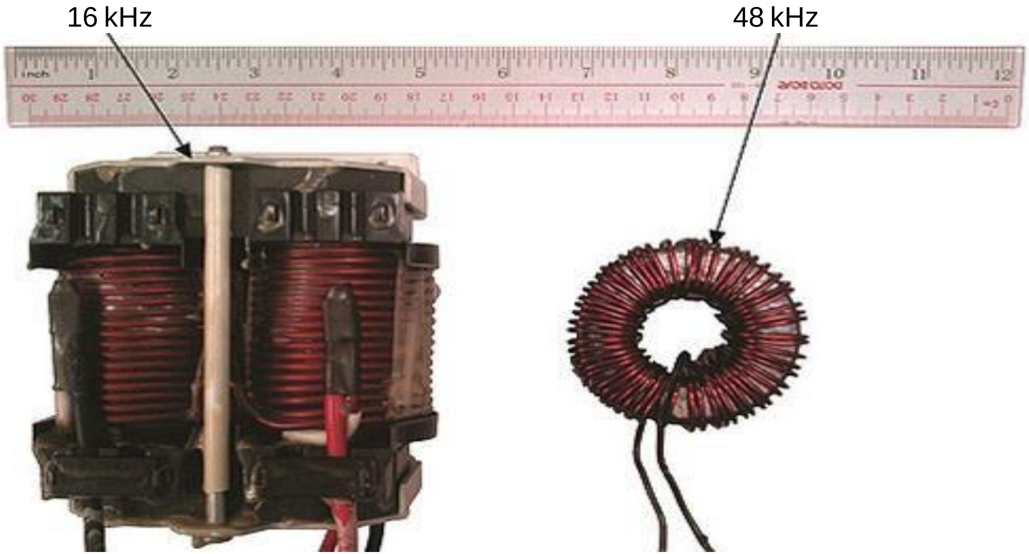
Estimated % Material Cost Breakdown

- 🟥 Power Modules
- ■ Controls
- 🟩 Housing & Heatsink
- 🟩 Magnetics
- 🟨 Capacitors
- 🟪 SMPS & Components
- 🟪 EMI Components



Solar Applications: Why is SiC a Good Fit?

Effects of Switching Frequency on a 30 A Boost Inductor



At 48 kHz

- Cost = 55% reduction
- Weight = 60% reduction
- Volume = 65% reduction
- Losses = 19% reduction

Compared to 16 kHz solution

Summary

☐ **1.To gain a Competitive Edge**

–High efficiency, reduce system space and light weight

☐ **2.Easier to achieve performance indicators**

-EMC/Noise/Efficiency/Heat dissipation

☐ **3.There are more and more successful cases and new application**

-Current trends

☐ **4.SiC can be used as a market segment, differentiation and product highlights**

-High-end products

Thank You

Questions

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