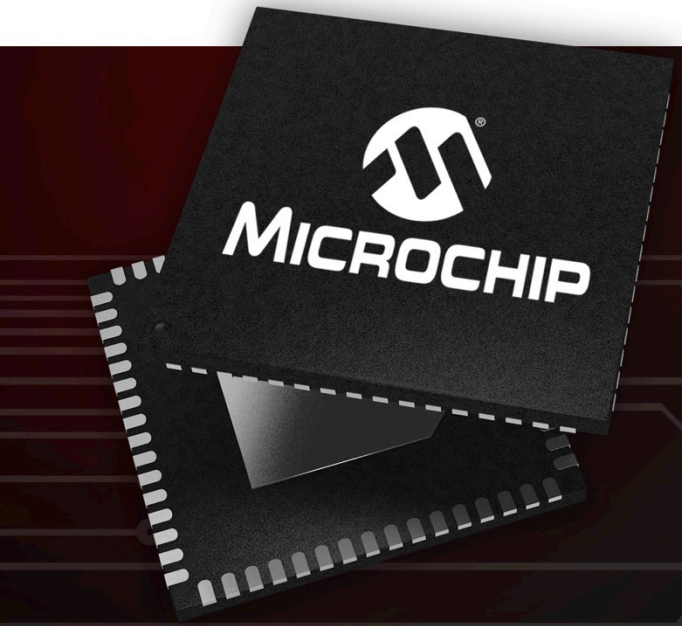
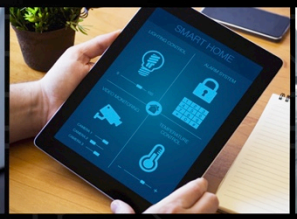
MICROCHIP




A Leading Provider of Microcontroller, Mixed-Signal, Analog & Flash-IP Solutions





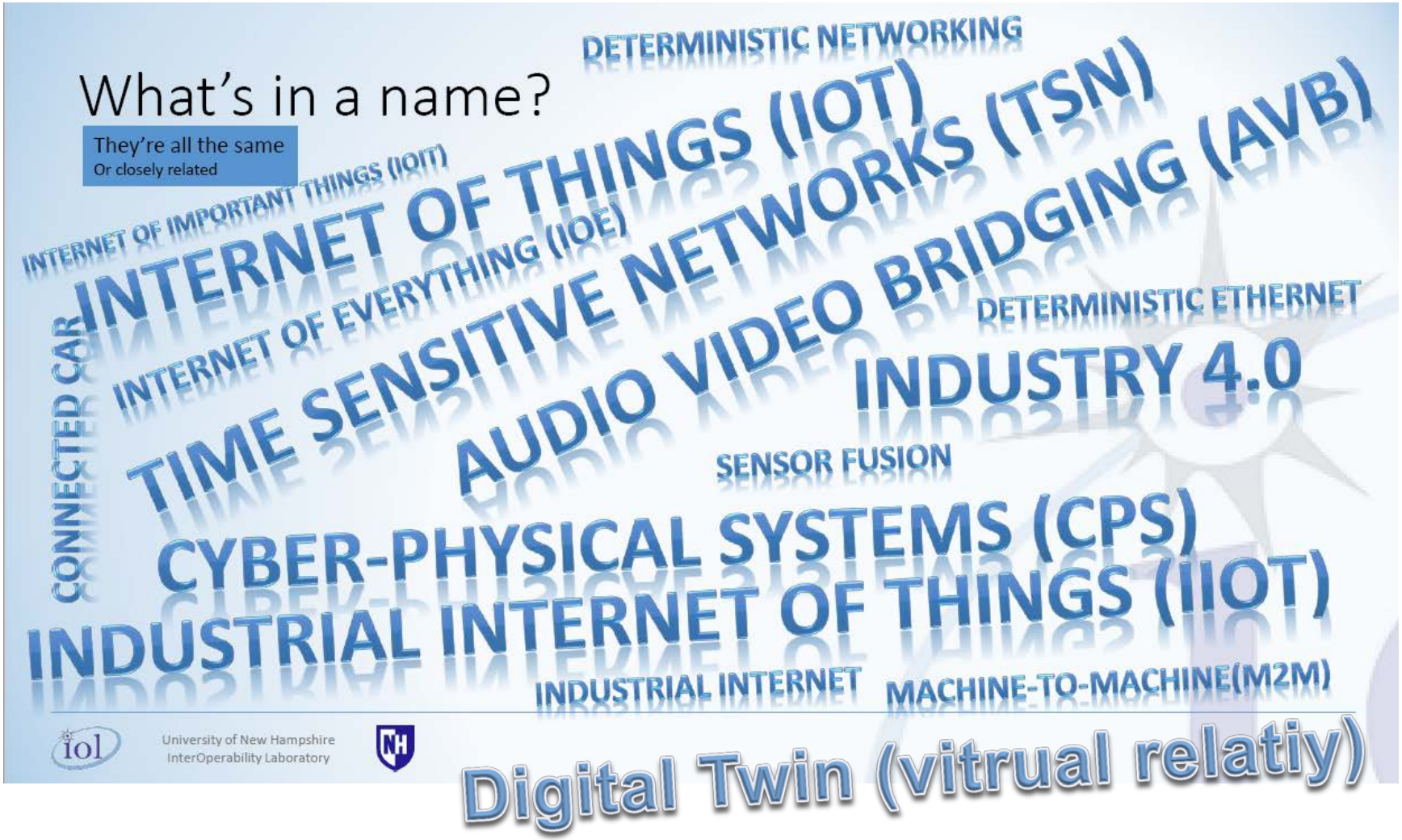

# Synchronization in industrial 4.0
# IEEE1588, redundancy and EtherCAT®

***Presented by: Lichien Hu***


# Synchronization in industrial 4.0 IEEE1588, redundancy and EtherCAT®

***Presented by: Lichien Hu***
***Microchip Field Applications Engineer***

# You May Hear the Following

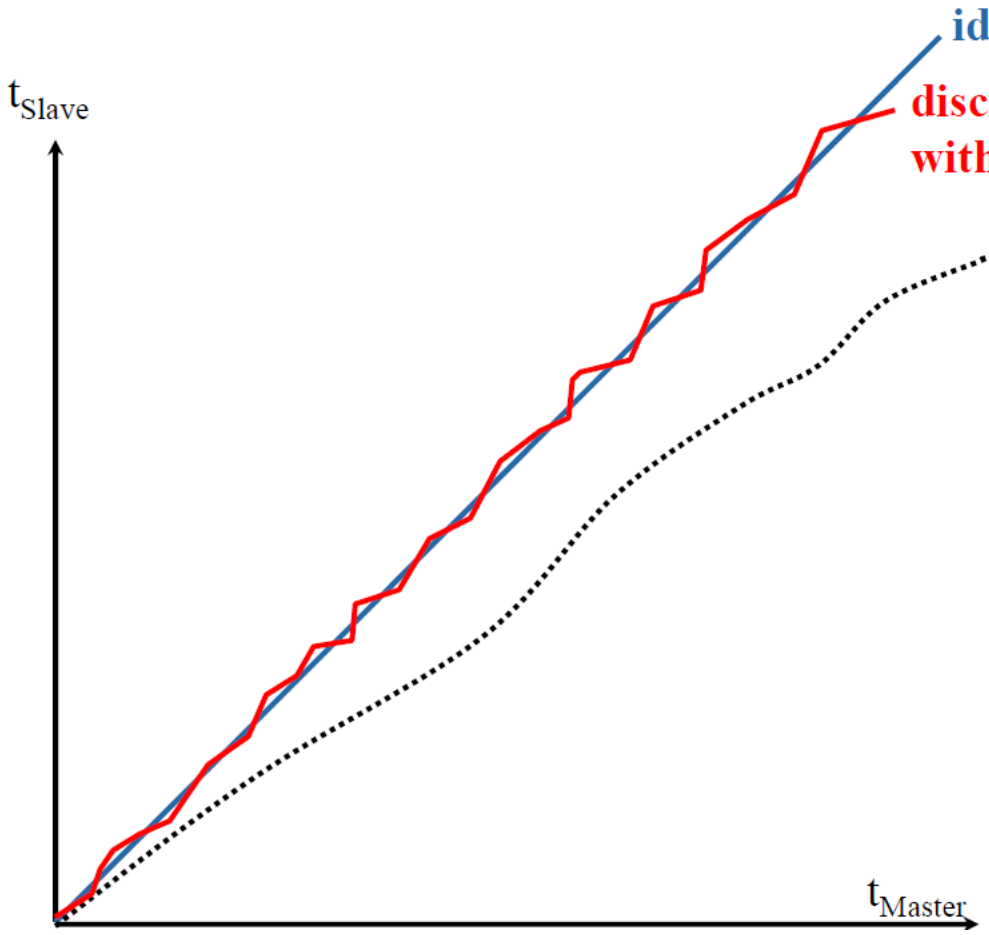


# Why Synchronization?

*“A man with a watch knows what time it is.*
*A man with two watches is never sure.”*

— Segal’s Law

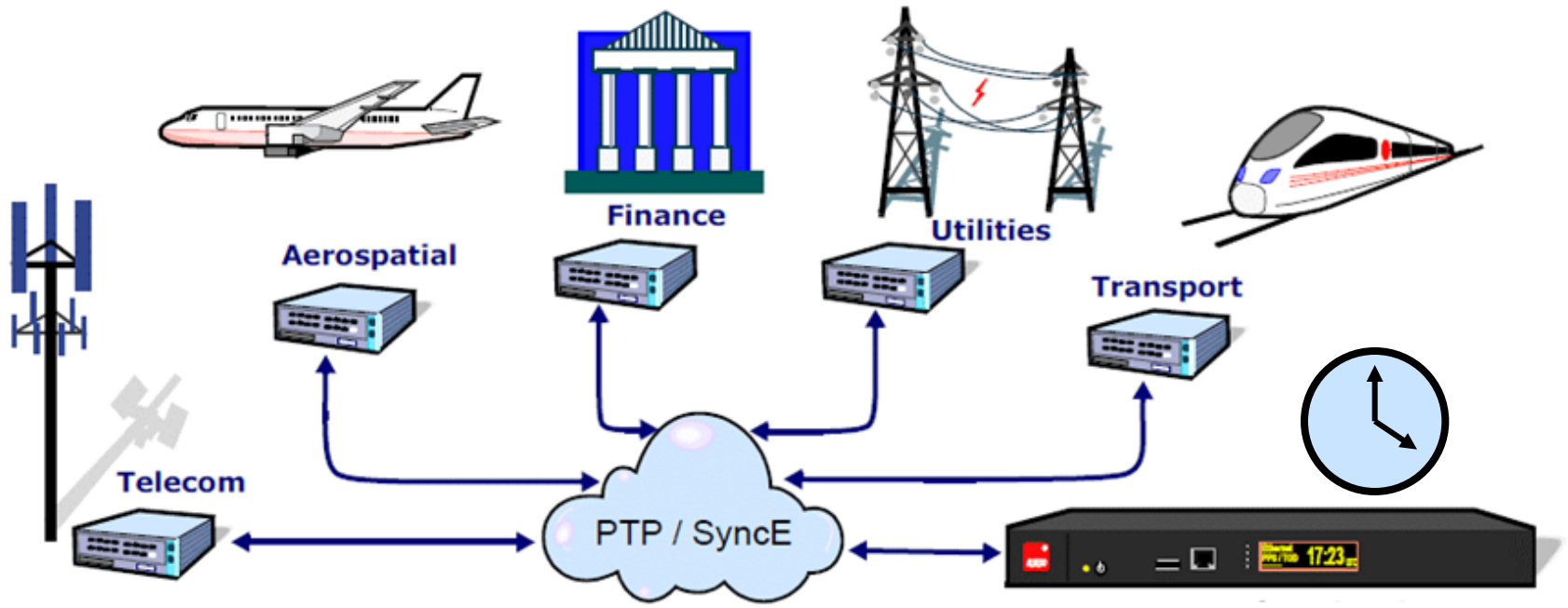
# Effect and Limitations of Clock Adjustment




**free running : the slave's oscillator**

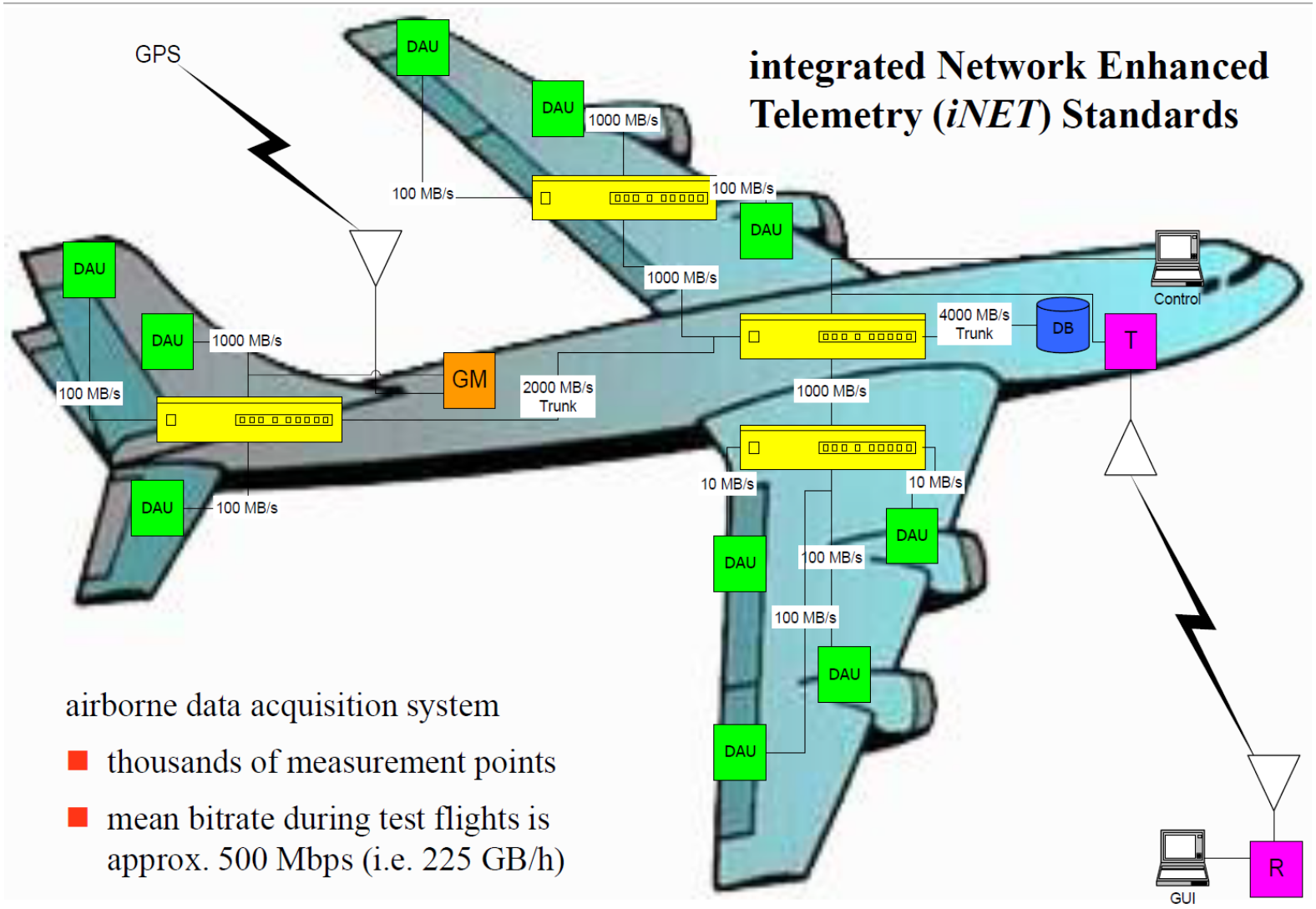
- **is in this example on average a little bit too slow (difference between nominal and effective frequency)**
- **its drift (phase change rate) varies with time (subject to temperature, acceleration, ageing, etc.)**

# Where is It Used (Applications)?



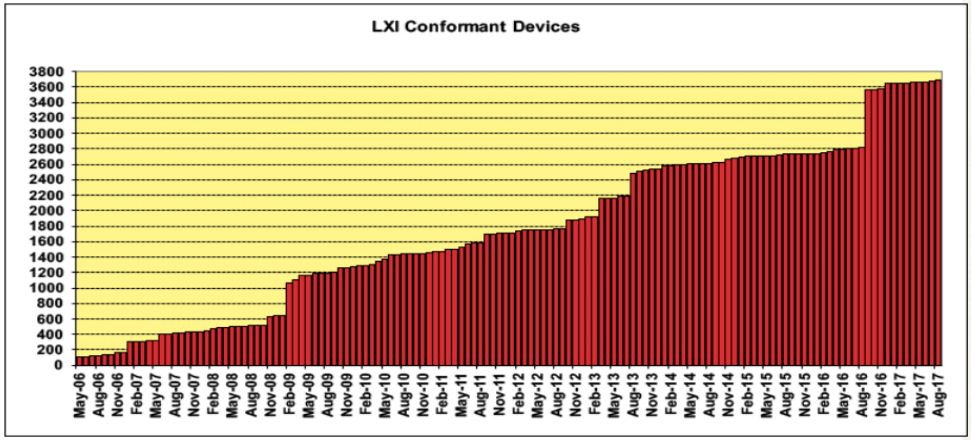

- **Distributed, real time control and data acquisition needed**

# Data Acquisition

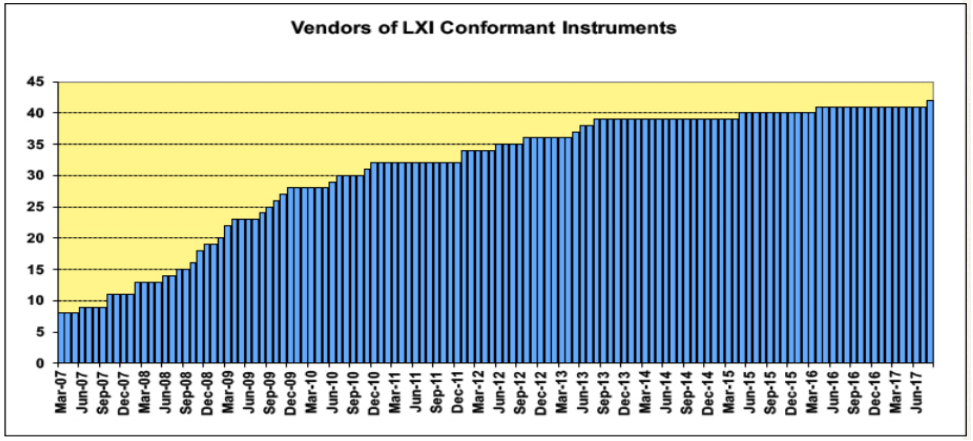


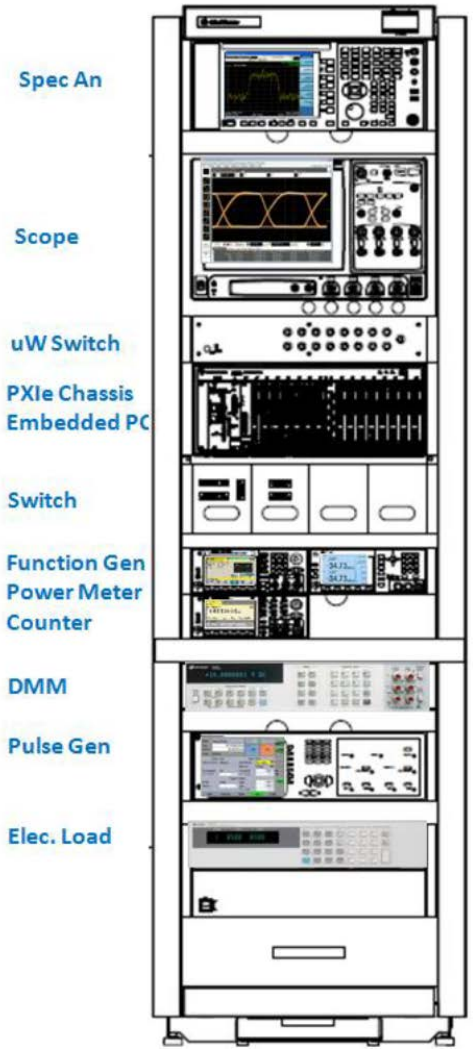
# LXI

- **LXI : LAN extension instrument based on IEEE1588**




Growth of Vendors of LXI Conformant Instruments



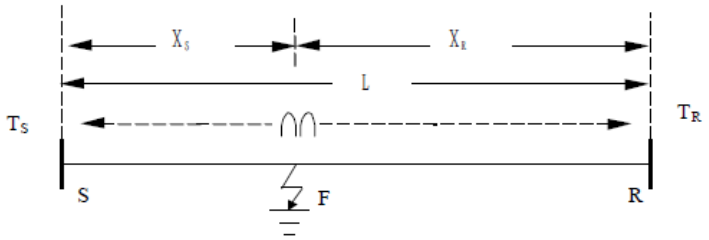
# Smart Grid Application

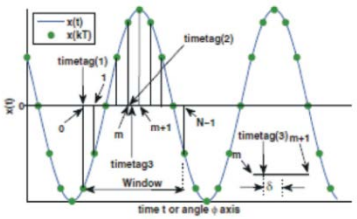
- Timing synchronization in power system consider in 4 categories：
  - Less than 1μs：Traveling wave / light arrest fault allocation, EDI pharos sync (MPU) for power quality monitoring (smart grid)
  - Less than 1ms：Fault recorder、and protection relay
  - Less than 10ms ：FTU、TTU、Smart grid power distributor
  - 1 sec or above: SCADA

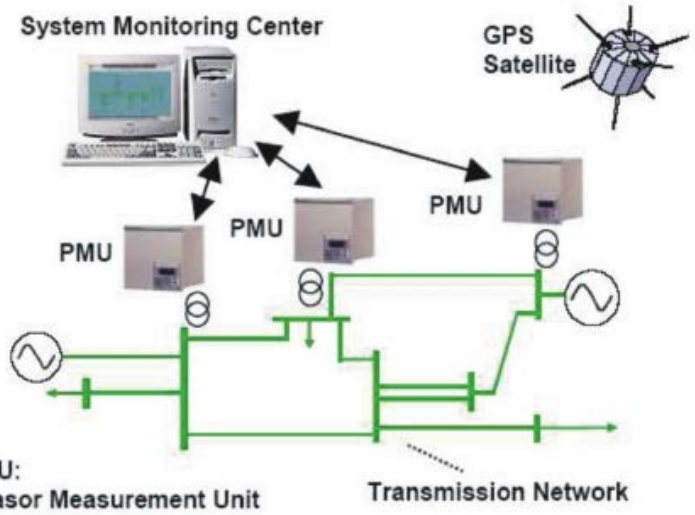
| Application | Standards | Required Accuracy |
|---|---|---|
| Synchrophasors | IEEE C37.118.1/2 -2011 | 1 μs |
| Line Differential Protection | | 1 μs |
| Sampled Analog Values | IEC 61850-7-2 (Service Models)<br>IEC 61850-9-2 (Mapping to Layer 2 /Ethernet) | 1 μs |
| SCADA System | | 1 ms |

$$X_S = [(T_S - T_R)\cdot v + L]/2 \qquad (3.a)$$

$$X_R = [(T_R - T_S)\cdot v + L]/2 \qquad (3.b)$$



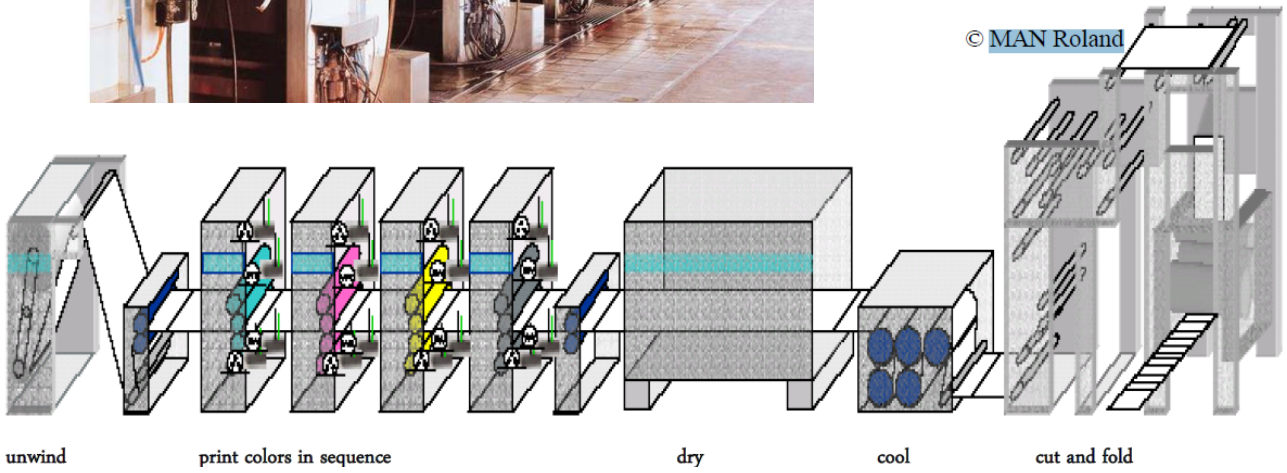



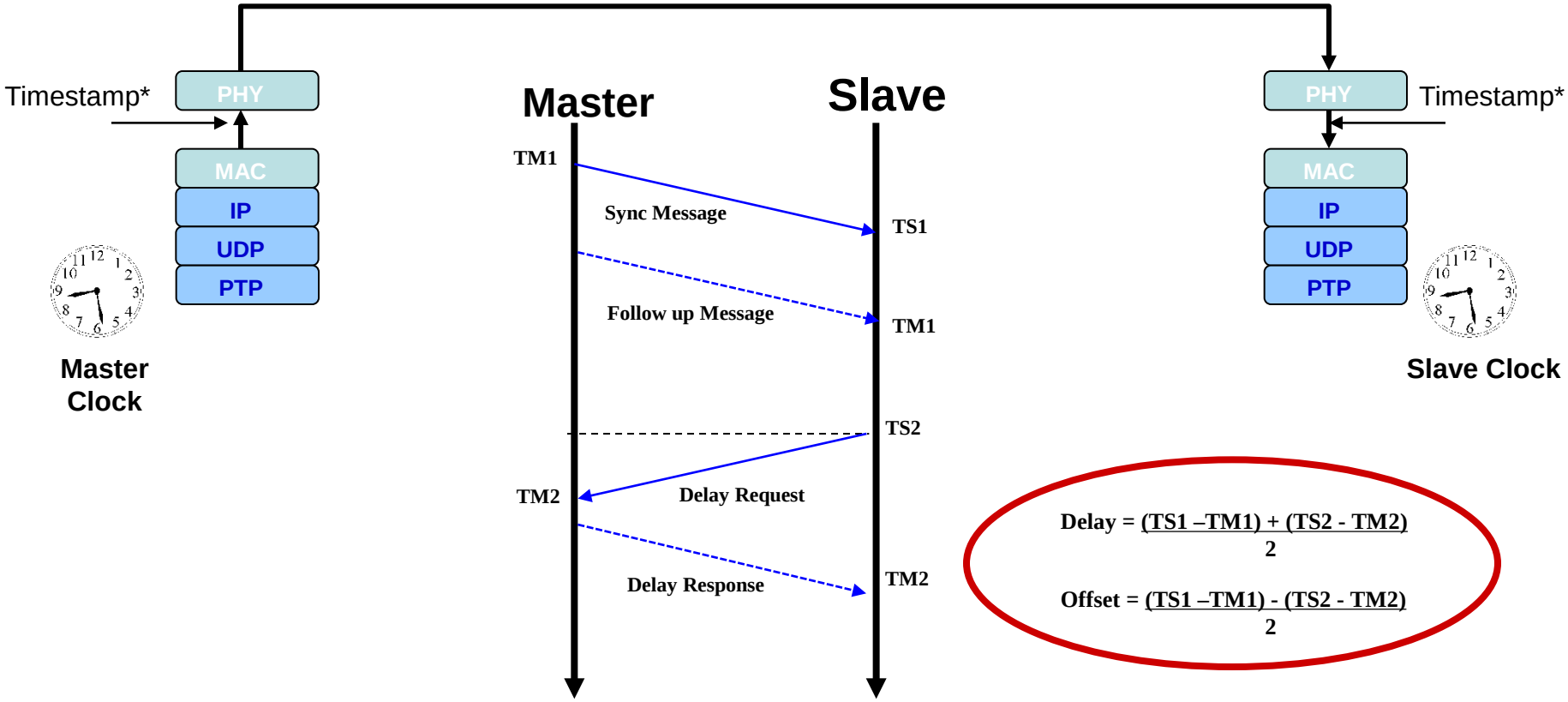

**1us= @ light speed =300m = 0.018º phase angle @ 50Hz**

# Industrial Control
## Example: Digital color offset printing

- speed up to v = 20 m/s
- printing accuracy Δs = ± 5 µm
- synchronization requirement: Δs/v = ± 250 ns




# Basic IEEE1588 / 802.1AS Synchronization

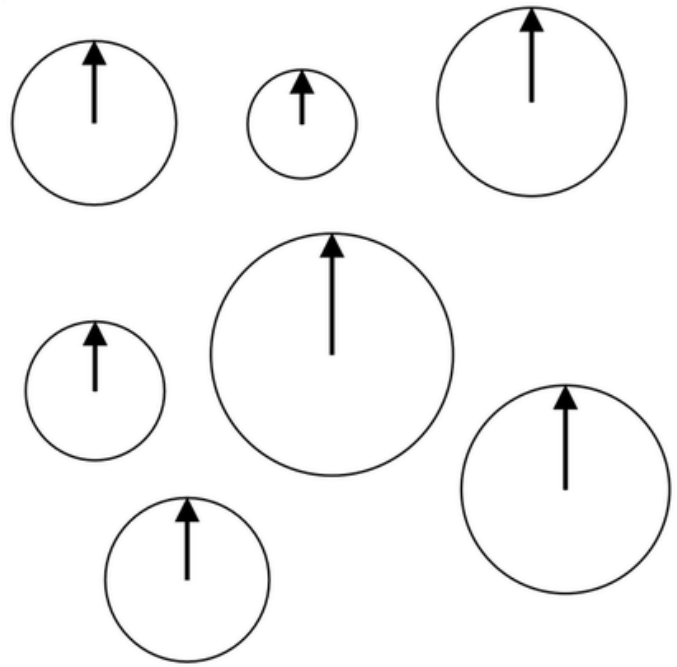



- 2-Step method example using follow up message.
- 1-Step method adds master nodes egress timestamp to Sync Message ‘on the fly’, eliminating the need for follow up message.

*** Timestamp as close as possible to line to remove variable delays**

# Time Synchronization with EtherSynch®

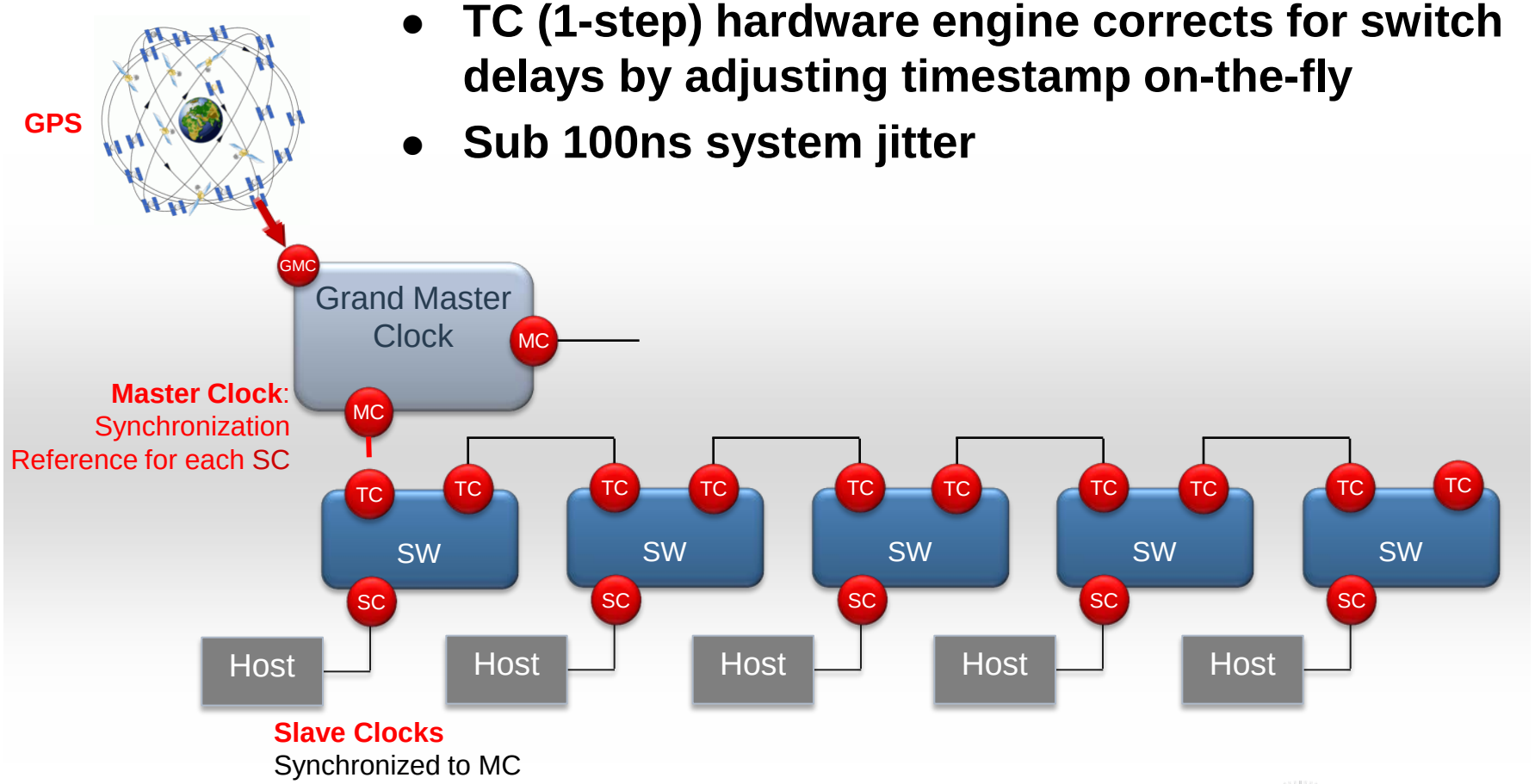
- **Supports ALL standards and features**
  - IEEE 1588-2008 Precision Time Protocol and IEEE 8021.AS (gPTP)*
  - Boundary or Transparent Clock with auto (hardware) correction
  - Master and slave Ordinary Clock
  - End-to-end and peer-to-peer
  - 1 and 2 steps
  - Multicast and unicast messaging
  - IPv4/v6 and IEEE 802.3
  - Packet filtering
  - Synchronous Ethernet via recovered clock



* Part of AVB (Audio Video Bridging)

# EtherSynch® Clock Synchronization

- **TC (1-step) hardware engine corrects for switch delays by adjusting timestamp on-the-fly**
- **Sub 100ns system jitter**



# What is Ethernet AVB?
## (Audio Video Bridging)

- **Supports audio & video (real-time) content over (packet based) Ethernet network**
- **Definable latencies and QoS even during congestion**
  - Guaranteed maximum 2ms delay over 7 hops
- **Supports synchronized play back across many nodes**
  - Talker / Listener concept
- For AVB to ‘really’ work it must be a defended network

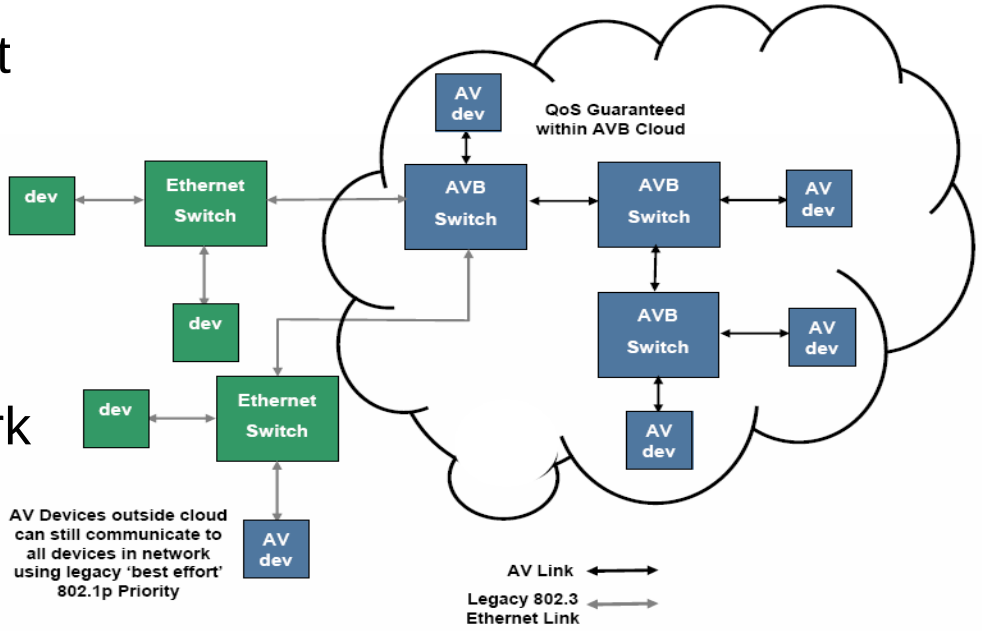



Figure 9. AVB Cloud

# What is TSN?

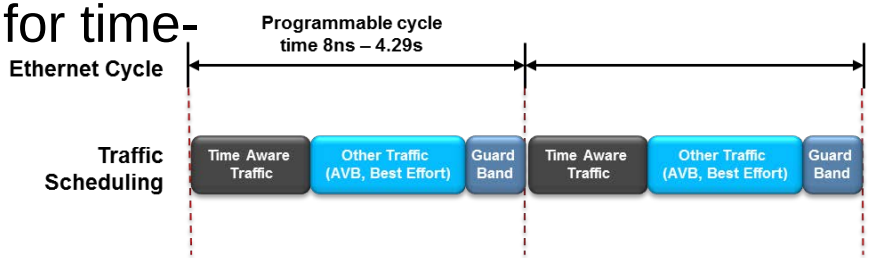
- **Originally AVB Gen 2 renamed to 'Time Sensitive Networking'**
  - More appropriate – not just A/V but stringent time critical control
- **TSN is a collection of many specs → 'TSN toolbox'**
  - Select the necessary tools (specs) for the required task
- **Specs include (continue to grow!)**
  - 802.1Qbv – Time Aware Scheduling
  - 802.1Qbu – Frame Pre-emption
  - 802.3br – Interspersing Express Traffic
  - 802.1Qch – Cyclic Queuing & Forwarding
  - 802.1Qci – Ingress Policing
  - 802.1Qca – Path Control & Reservation
  - 802.11CB – Seamless Redundancy

**And there's more coming !**

# EtherSynch® Deterministic Switch Engine

- **AVB (Audio Video Bridging)**
  - Time synchronization, Stream Reservation, Traffic Shaper

- **Time Aware Traffic Scheduler (Draft 802.1Qbv)**
  - Periodic scheduling reserved for time-critical class traffic
  - Time sensitive Control



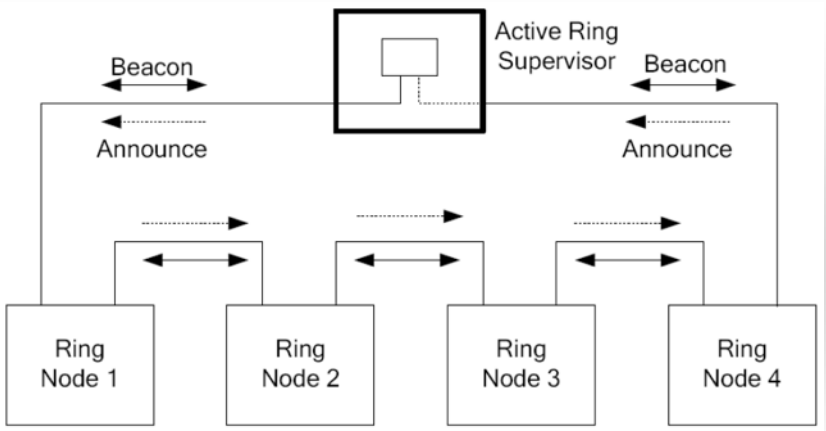

- **Low Latency**
  - 'Smart' cut-through Time-Aware traffic forwarding
  - 64-byte 'store-and-stream'
  - 10X Switch latency reduction
    - Eg.<1uS for GigE

Time-Sensitive Networks (TSN)

# Network Fault Recovery (DLR)

- **Device Layer Ring (DLR)**
  - Ring Supervisor and Ring Node support
  - Store / send programmable periodic Beacon frames (supervisor)
  - Loss of Beacon packet detection (supervisory & node)
  - Fast flush MAC table entries
  - Free library available via product page

- Ring topology
- Beacon based fault detection
- Single fault switchover redundancy

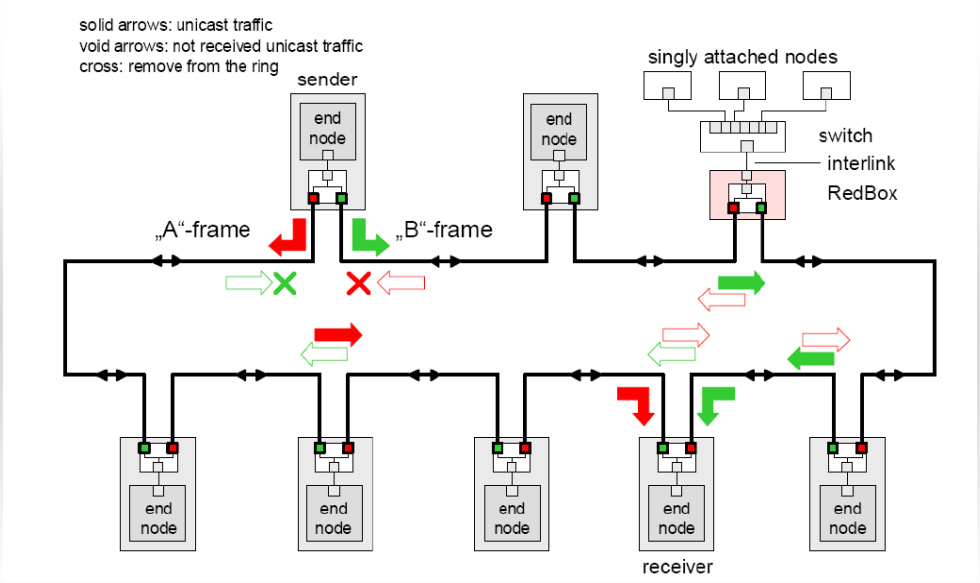


# Network Fault Recovery (HSR)

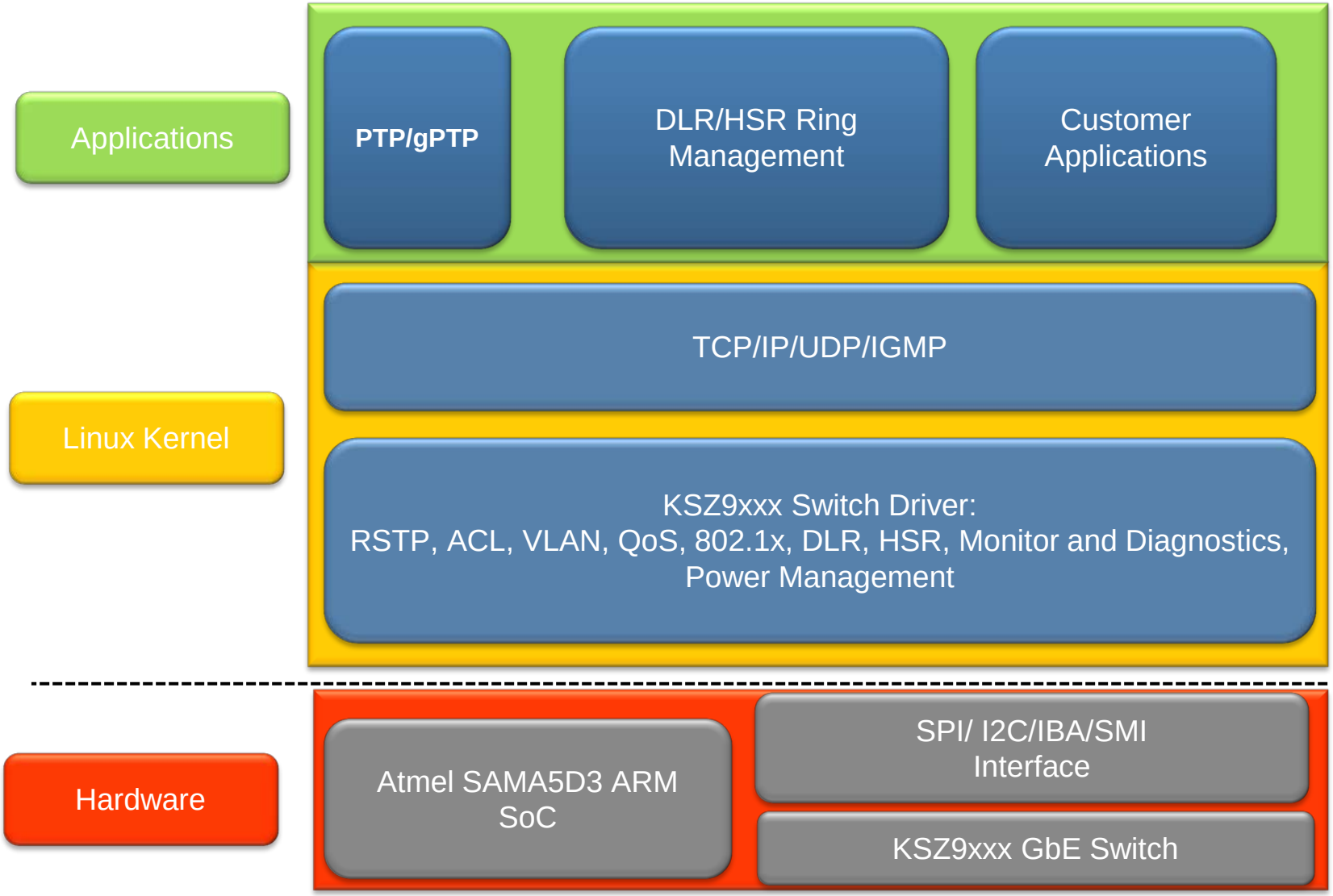
- **High Seamless Redundancy (HSR)**
  - HSR packet duplication
  - Duplicate HSR packet discard
  - 256 HSR node ring support
  - Free library available via product page

**IEC 62439-3 Cl. 5**
HSR - High-availability Seamless Redundancy

- Ring topology
- Duplicated packet redundancy
- Single fault seamless (instant) switchover



# EVB Software Stack



# 3-Port 10/100 Switch Selector

| Product | KSZ8863 | KSZ8873 | KSZ8463 | LAN9303 | LAN9353 | LAN9354 | LAN9355 |
|---|---|---|---|---|---|---|---|
| Ethernet Bandwidth | 10Base-T/ 100Base-TX /100Base-FX | | | 10Base-T / 100Base-TX | 10Base-T/ 100Base-TX /100Base-FX | | |
| Interface | MII / RMII | | | | | RMII | MII |
| Wake-on-LAN | | | Yes | | Yes | Yes | Yes |
| EEE | | | Yes | | Yes | Yes | Yes |
| Vdd IO | 1.8/2.5/3.3 | 1.8/2.5/3.3 | 1.8/2.5/3.3 | 3.3 | 1.6-3.3 | 1.6-3.3 | 1.6-3.3 |
| LinkMD Cable Diag | Yes | Yes | Yes | | Yes | Yes | Yes |
| IEEE 1588 | | | Yes | | Yes | Yes | Yes |
| Power Consumption* | 520mW Total | 520mW Total | 330mW Total | 640mW Total | 555mW Total | 555mW Total | 555mW Total |
| Packages | 48/LQFP | 64/LQFP | 64/LQFP | 56/QFN | 64/ QFN, 64/ TQFP | 56/ QFN, | 88/ QFN, 80/ TQFP |



* Includes Transformer

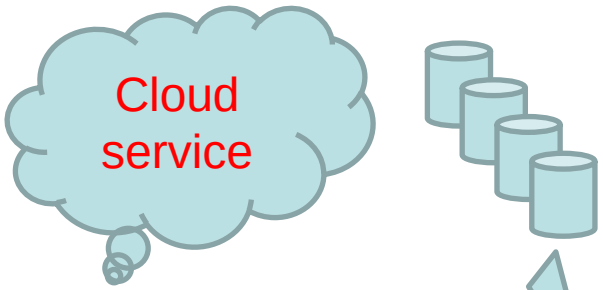
# AVB Switch Software Enabled Features

| Feature | KSZ989x 10/100/1000 | KSZ856x 10/100 | KSZ956x 10/100/1000 | KSZ947x 10/100/1000 | Comments |
|---|---|---|---|---|---|
| **Linux® Driver** |  |  |  |  | Supports 802.1X, ACL, RSTP |
| **PTP/gPTP** Precision Time Protocol | |  |  |  | IEEE 1588 v2 and 802.1AS Linux Library |
| **AVB** Audio/Video Bridging | |  |  |  | Open-AVB Linux Library |
| **Time Aware Scheduler** | |  |  |  | IEEE 802.1Q Linux Library |
| **Device Layer Ring** (DLR) | | | |  | DLR Linux Library |
| **High-Availability Seamless Redundancy** (HSR) | | | |  | HSR Linux Library |
| **DLR/HSR Management** | | | |  | Protocol facilitating passing of node status to Host |

x = Number of Ports (3 to 7)

# Microchip IoT View

RESTFUL /JSON SUPPORTED

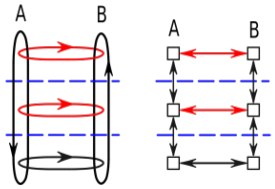



AWS
AZURE
IBM
SQL.

**ML**
**Data Visualization**
**Big data analytic**

**Crypto**

TSL/SSL
ECC
Asymmetric
crypto




**Protocol**

COAP
MQTT
RLP

**Connectivity**

Short range

**BT**
**Wi-Fi**
**Zee Bee**

Long range

**Lora**

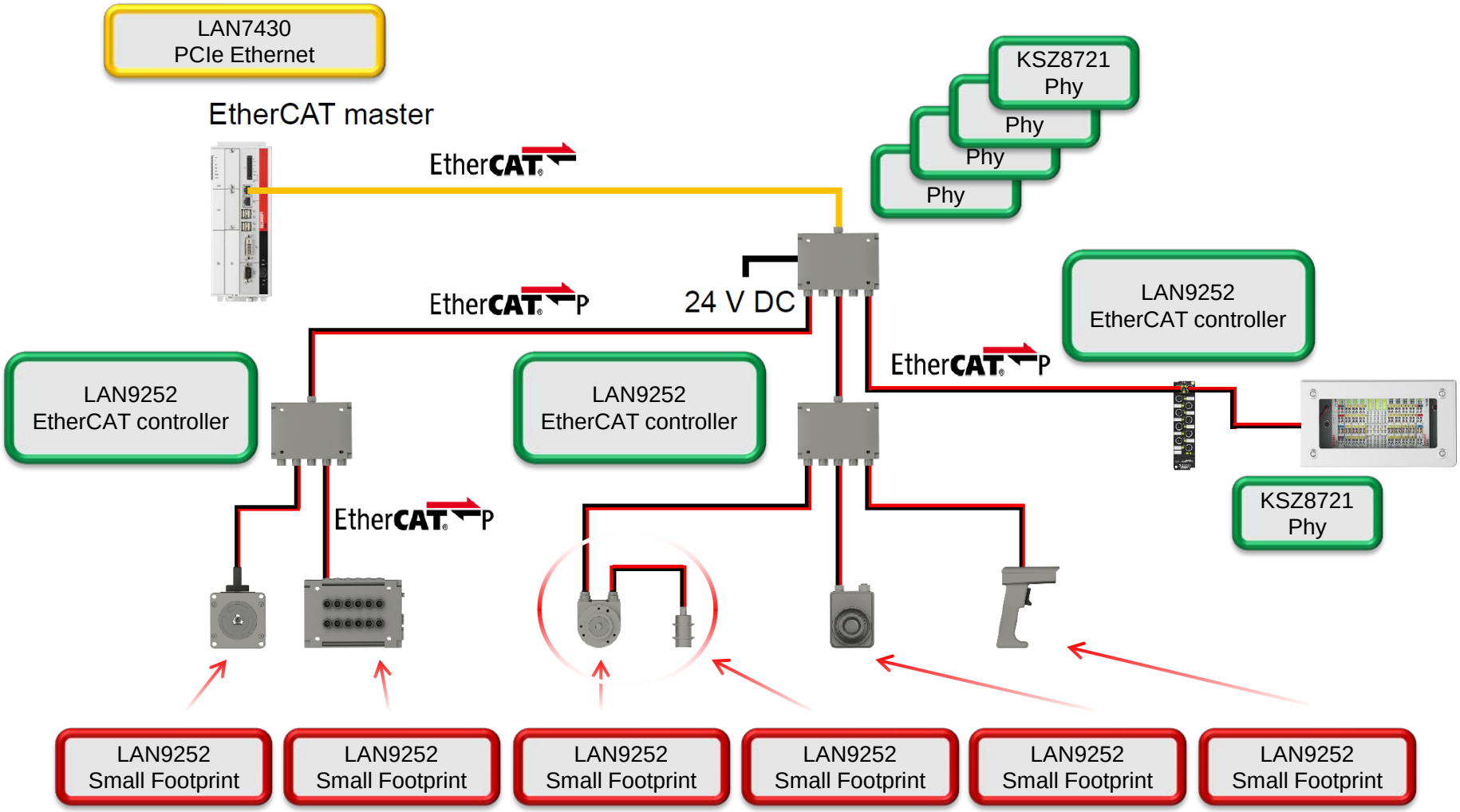
Wire

**USB**
**LAN**

# EtherCAT® Synchronization

- Distributed clock is a synchronization method in EtherCAT
- Total 64-bit
- Microchip's LAN9252 is a EtherCAT slave controller, it supports DC
- Use Sync & Latch pin and DC unit to sync with each slave node

# EtherCAT® - Where It Fits?



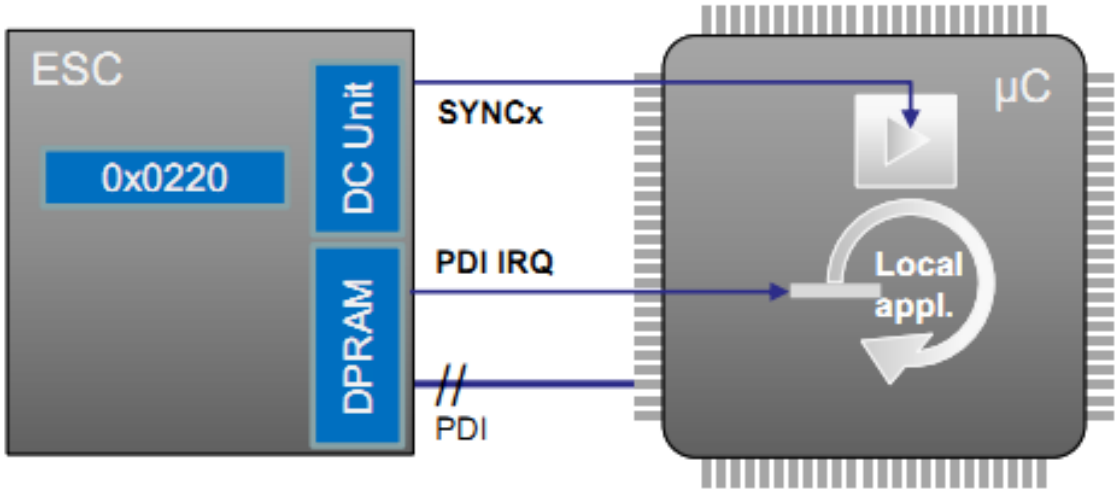
# DC And Synchronization

- **Distributed clock (DC) in EtherCAT is to sync each salve node to a common clock , normally, the first slave's time as the Reference clock**
- **DC provide following functions**
  - System time ： From 2000.1.1+500 yeas(64-bit @ "ns" ) Or 4.2S (32-bit @ "ns" )
  - Reference clock
  - Calculation drift, compensation, wire delay offset ..
- **DC can sync each slave's OUTPUT/ INPUT into different synchronization modes**
  - No Sync →Free Run
  - Sync with Jitter →Sync to Sync manager
  - Precise Sync → Sync to DC

| 同期模式 | 内容 | 同期方法 | 特征 |
|---|---|---|---|
| DC | SYNC0 事件同期 | 以第 1 轴的时间为基准<br>同期其他从站的时间信息 | ・高精度<br>・需要在主站侧进行补偿处理 |
| SM2 | SM2 事件同期 | RxPDO 的收信时间同期 | ・没有传送延时补偿精度差<br>・一定要在上位控制器侧保证传送时间<br>（专用的硬件等） |
| FreeRun | 非同期 | 非同期 | ・处理简单<br>・欠缺实时性 |

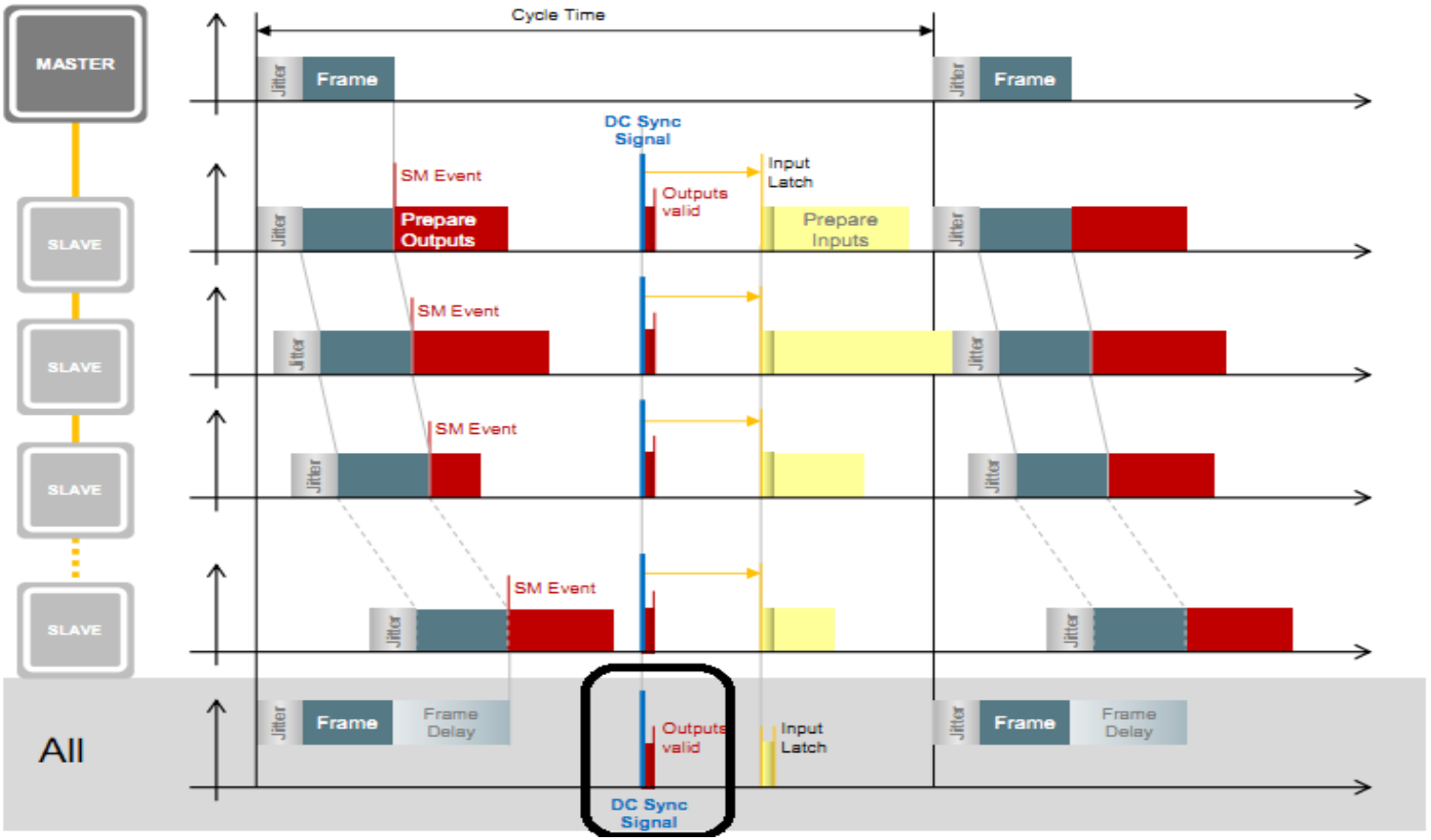
# Synchronization with SOC

- Synchronization with Distributed Clock
  - Local application in µC can be triggered by PDI IRQ or polling the SM-Event Register
  - Setting of Outputs or latching of inputs shall be triggered by Sync0-Signal from ESC



# Synchronization - Enabled

- With Sync enabled, outputs valid from each slave at same time.
- Precise synchronization achieved between all slaves (<<1us)



# Ethernet Products


**Experience**

***Maximum Reliable Bandwidth***

**with Ethernet …**

***Transceivers (PHYs)***

***Controllers***

***Bridges***

***Switches***

# EtherCAT® Industrial Solution


- **Single packet, multiple nodes – reduces bandwidth overhead for simple data transfers**
- **Standard Ethernet packet – connects to existing Ethernet networks without special cables, routers or switches**
- **High-accuracy distributed clocks – done in hardware with register settings, no software overhead**

EtherCAT®


# To Be Continued…
# Time Sensitive Network


# Thank You!
# Any Questions?

# Microchip Resources

**Microchip 工程師社區** http://www.microchip.com.cn/community

快訊 http://www.microchip.com.cn/community/html/newsletter.shtml

Weibo.com/microchiptech

t.qq.com/microchiptech

http://i.youku.com/Microchip

https://www.youtube.com/playlist?list=PLEB6441B0D29C405B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- 高雄 (07) 213-7830
- 台北 (02) 2508-8600

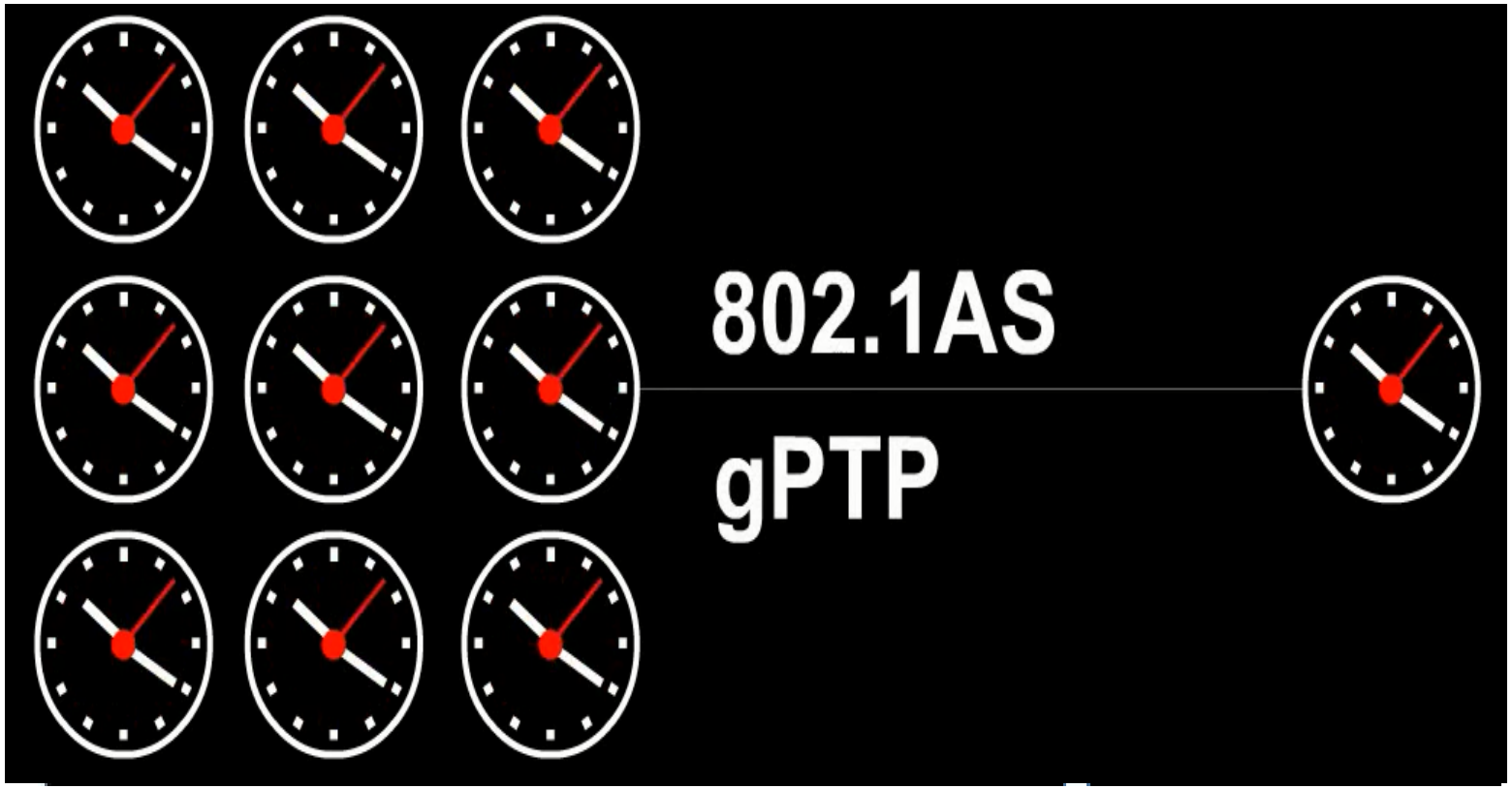

# Additional Slides

# V1 / V2 difference

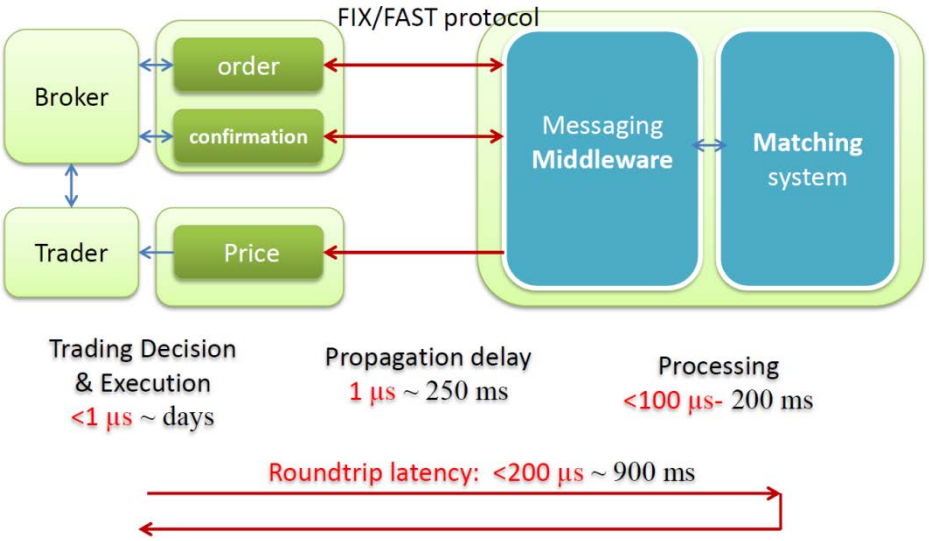
| Criteria | PTPv1 | PTPv2 |
|---|---|---|
| clock types | Ordinary Clock (OC)<br>Boundary Clock (BC) | Ordinary Clock (OC)<br>Boundary Clock (BC)<br>end-to-end Transparent Clock (e2e TC)<br>peer-to-peer Transparent Clock (p2p TC)<br>Management Node |
| time representation | epoc number (16 bit)<br>seconds (32 bit)<br>nanoseconds (32 bit) | <br>seconds (48 bit)<br>nanoseconds (32 bit) |
| time interval resolution | 1 ns | $2^{-16}$ ns (15.26 fs) |
| message types | <br>Sync<br>Follow_Up | Announce<br>Sync<br>Follow_Up |
| | Delay_Req<br>Delay_Resp | Delay_Req<br>Delay_Resp |
| | Management | Management |
| | | Pdelay_Req<br>Pdelay_Resp<br>Pdelay_Resp_Follow_Up |
| | | Signaling |
| message rates | small choice | bigger range and selectable per message type |
| addressing | multicast | multicast<br>unicast |
| mappings | UDP/IPv4 over IEEE 802.3 | UDP/IPv4 over IEEE 802.3<br>UDP/IPv6 over IEEE 802.3<br>directly over IEEE 802.3<br>PROFINET<br>DeviceNet/ControlNet |
| extensions | none | by Type/Length/Value (TLV) |
| redundancy | BMC | BMC, Alternate Master, Master Cluster |
| | no | yes |
| multiple domains | by 4 multicast addresses | by Domain Number (8 bit) |
| What else? | | profiles |
| | | unicast message negotiation |
| | | security protocol (experimental) |

Table 1: PTPv1 / PTPv2 comparison

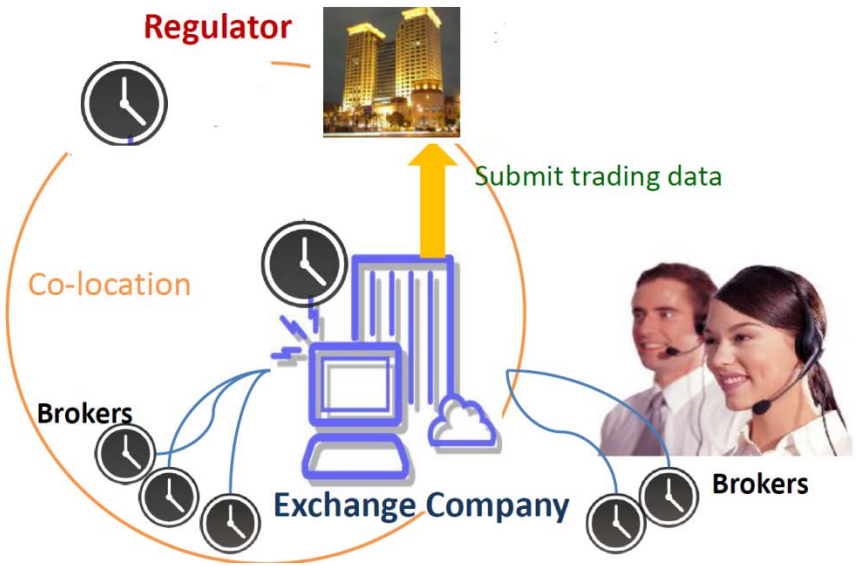
# What That Means



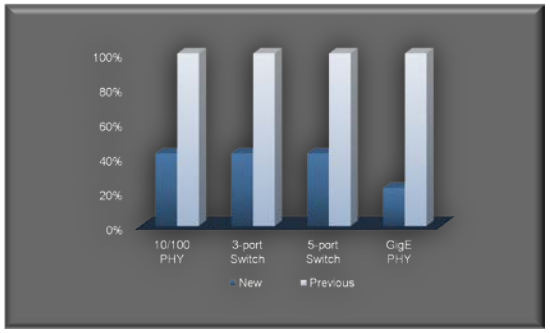
# Stock Market Application



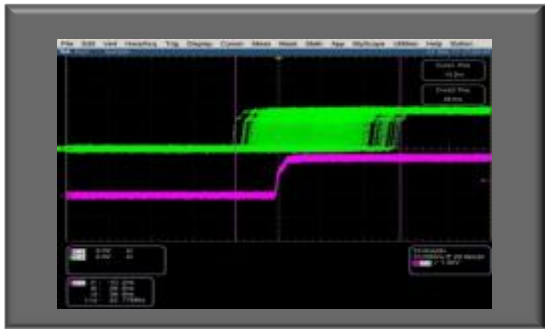




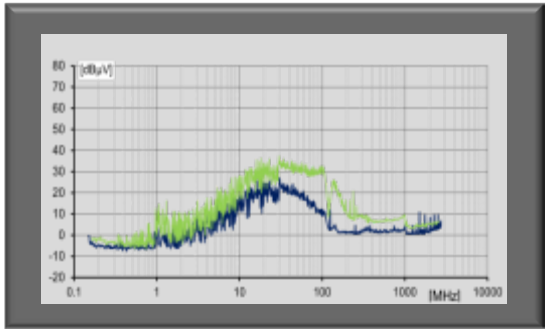
# Advanced Ethernet Technology




- **Energy Efficiency**
  - Ultra-Low Power, Patented Ethernet PHY
  - EtherGREEN™ Platform Advanced Power Management
  - Ultra-Deep-Sleep uA Standby



- **Deterministic**
  - EtherSynch® Platform IEEE 1588v2/802.1AS Synchronization
  - Fixed / Low-Latency Transmission
  - AVB / Time-Aware Traffic Scheduling




- **Reliability**
  - Quiet-WIRE® Technology Enhanced EMC Performance
  - LinkMD®+ Diagnostics (Link Quality Indicator)
  - Network Fault Recovery Hardware Engine

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# Trademarks