AndesSight™
Software Developer’s Environment

General Description

AndesSight™ is an Eclipse-based integrated development environment (IDE) which provides an efficient way to develop embedded applications for AndesCore™ based SoCs.

Features

AndesSight™
- Eclipse-based IDE
- Project management
- Managed build system
- Feature/func editor
- Source level debugger
- Profiling analysis
- In-System programming
- RTOS awareness debugging
- Break and display on exceptions
- Register list/stack viewing and update
- Multicore development support
- Custom UI
- AndesCore™ V5 CPU support
- Extensive demo projects
- Flexible license control
- Corvette™ (Arm-Compatible board) support

Compilation Tools
- Compiler
- Assembler
- Linker
- Library
- Build/Analysis

Debug/Analysis
- Debugger
- Profiler
- Memory
- Code Coverage
- Code Size
- Code Analysis

Target Systems
-(114,565),(733,657)
- In-Circuit Emulator (ACE)
- Virtual Emulator Platform

AndesSight™ IDE
- Managed Build System
- Debugger Interface
- Target Management

Toolchains
- Compiler for Linux and Windows
- Andes efficient ROM patch solution
- Highly optimized DSP library functions
- Highly optimized micro functions

Simulator
- CPU simulator
- Memory/cycle accurate
- Model of AndesCore™ SoC platform

ICE
- ACE/C, debugger (4-wire/2-wire)
  with OpenGCD support

Supported Host Platforms
- Windows 7 / Windows 10
- Ubuntu: Linux 18.04 / 16.04 / FreeBSD 11.0 / Red Hat Linux 6.6

About Andes Technology

Andes Technology, the first CPU IP supplier in Asia, has been devoting to the development of innovative high-performance RISC-V microprocessors and associated SoC platforms since its foundation in 2003. Its powerful CPU groups covering arm@26, mid-range, high-end, accessible and security families has achieved design wins in numerous embedded applications across the world, making a cumulative record of over 5 billion SoC shipment containing Andes IP up to 2019. While delivering advanced features based on proprietary ISA, As a Founding Premier member of RISC-V International Association, Andes is also the first mainstream CPU vendor adopting the open RISC-V. For more information about Andes products, technologies and services, please contact us through the following:

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Two AndesSight™ Versions:

STD
A comprehensive IDE with highly-optimized compilers, all GUI features, and Linux support.

RDS
Based on AndesSight™ STD with additional customization features for customers’ redistribution.
AndesStar™ Architecture

The AndesStar V8L, the latest member of Andes architecture, consists of both 32-bit and 64-bit register architectures with mixed-length 1632-bit instructions. It adopts the RISC-V technology as its subset and benefits from the fast growing RISC-V ecosystem. Together with the benefits of power enhancement extensions segregated from V3, the third generation RISC-based architecture, the AndesStar V8 brings compact, modular and customizable advantages to SoC applications. As a Founding Premier member of the RISC-V International Association, Andes is determined to take RISC-V to the mainstream.

AndesShape™

AndesShape™ development platform includes variety of software hardware entities, such as pre-integrated CPU core SoC platform (IPA, ICE debugger (AICE), and hardware evaluation boards for AndesCore™ processor based system development. To satisfy the best quality-of-result (QoR) requirements for different system applications, various platform IPs are available with different bus and datapath structures. In addition to a basic set of connectivity and storage devices, the rich set of hardware options in both board and SoC levels enable versatile flexibility in hardware/software co-development and early prototyping.

The comprehensive debugging support, including in-system programming, self-diagnosis, and embedded ICE, greatly reduces the system development cycle while maintaining the quality of designs.

AndesSoft™ Building Blocks for System - AndesSoft™ Software Components

With the AndesShape™ platform, Andes users can develop software with hardware in a seamlessly integrated environment efficiently, to speed up the development process. Andes further provides a rich set of software components, from Real-Time Operating System, Linux kernel and drivers, libraries, and middleware, to application frameworks, running on AndesCore™ processors under the name AndesSoft™. Users can leverage these well-prepare and verified building blocks based on their needs and focus on tackling products to greatly improve time-to-market.

AndesCore™: Performance, Power and Area

AndesCore™ is a high-performance, CPU core family geared to diverse market segments from today’s emerging embedded applications. AndesCore processors are based on the AndesStar™ V5 Instruction Set Architecture (ISA), which is compliant to the RISC-V technology. The versatile and non-invasive features of the AndesCore family allows flexible SoC customization based on the application needs in a design to improve platform performance and reduce system cost. In addition, the processors possess various, commonly-used low power design techniques to save energy and further allow smart SoC level power management, giving the AndesCore family better energy-performance outcomes.
AndesStar™ Architecture

The AndesStar™ V5, the latest generation of Andes architecture, consists of both 32-bit and 64-bit register architectures with mixed-length 1632-bit instructions. It adopts the RISC-V technology as its subset and benefits from the fast growing RISC-V ecosystem. Together with the benefits of partially enhanced extensions from V3, the third generation RISC-style architecture, the AndesStar™ V5 brings compact, modular and customizable advantages to SoC applications. As a Founding Premier member of the RISC-V International Association, Andes is determined to take RISC-V to the mainstream.

AndeSoft™ Building Blocks for System - AndeSoft™ Software Components

With AndeSoft™ IDE, users can develop software with hardware in a seamlessly integrated environment efficiently, to speed up the development process. Andes further provides a rich set of software components, from Real-Time Operating System, Linux kernel and drivers, libraries, and middleware, to application frameworks, running on AndesCore™ processors under the name AndeSoft™. Users can leverage those well-possibly and verified building blocks based on their needs and focus on tackling products to greatly improve time-to-market.

Fundamental

• Compiler and toolchain are contributed to and supported officially by GNU and LLVM communities
• Optimized C toolchain: MCC16b, newlib and glibc
• Optimized low-level compute libraries for NN, DSP and vector processing: libRtens, libfpe, etc.
• Condone linker script and its tools, Linker Scattering-and-Gathering (LiSaG)
• Bare-metal drivers and demo programs to demo AndesCore™ features
• Virtual Machine: AndesVM™ (32-bit architecture), AndesYS™ (SystemC library), Qemu

Real-Time Operating System

• Open source part on Andes. Zephyr, FreeRTOS
• Commercial port on Andes Core RTOS ThreadX, Ultras, RTThread, SysOS
• RISC-V ready: VXWorks, µC/OS-II, FreeRTOS, etc.

Linux, Middleware and SW Framework

• Linux kernel src-4.17 and LTS5.4, device drivers and advanced features: storage, trance, Perf, SMU, power throttling, suspend-to-RAM and kernel module
• U-Boot, OpenSSL and BIB
• Andes® connect Linux to IPv6 seamlessly

AndeShape™

The AndeShape™ development platform includes variety of hardware entities, such as pre-integrated CPU core SoC platform (APs, IEC Instrumentation (AICE), and hardware evaluation boards for AndesCore™ processor based system development. To satisfy the best quality-of-result (QoR) requirements for different system applications, various platform IPs are available with different bus and datapath structures. In addition to a basic set of connectivity and storage devices, the rich set of hardware options in both board and SoC levels enable various flexibility in hardware/software co-development and early prototyping.

The comprehensive debugging support, including in-system programming, self-diagnosis, and embedded ICE, greatly reduces the system development cycle while maintaining the quality of designs.

AndesCore™ AICE-MINH

AndesCore™ AICE-MCRO
Andes Technology, the first CPU IP supplier in Asia, has been driving the development of innovative high-performance low-power RISC-V architectures and associated SoC platforms since its foundation in 2005. Its powerful CPU cores covering entry-level, mid-range, high-end, serverable, and security families has achieved design wins in numerous embedded applications across the world, making a cumulative record of over 5 billion SoC shipments containing Andes’ IP up to 2016. While delivering advanced features based on proprietary RISC-V as a Founding Premier member of RISC-V International Association, Andes is also the first mainstream CPU vendor adopting the open RISC-V. For more information about Andes products, technologies and services, please connect us through the following:

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**Andes Core™**

A comprehensive IDE with highly-optimized compilers, all GUI features, and Linux support.

**Andes Core E™**

Based on AndesCore™ STD with additional customization features for customers’ redistribution.
Andes Technology, the first CPU IP supplier in Asia, has been devoting to the development of innovative high-performance RISC-V processors and associated SoC platforms since its foundation in 2002. Its powerful CPU IP portfolio covering microcontroller, microprocessor, high-end, embedded and security families has achieved design wins in numerous embedded applications across the world, making a cumulative record of over 5 billion SoC shipment containing Andes IP up to 2018. While delivering advanced features based on proprietary BIOS, as a Founding Premier member of RISC-V International Association, Andes is also the first mainstream CPU vendor adopting the open RISC-V. For more information about Andes products, technologies and services, please contact us through the following:

**Andes Core™**

**Andes Chipset**

**Andes Processor**

**Andes Technology**

**Andes Software**

**Andes System**

**Andes Security**

**Andes Cloud**

**Andes IoT**

**Andes Networking**

**Andes Industrial**

**About Andes Technology**

**Headquarters**

**Shanghai**

**USA**

**Shenzhen**

**Korea**

**Japan**

**Europe**

**Andes Technology Driving Innovations™**

**Andes Sight™**

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- In-System programming
- RTOS-aware debugging
- Break and display on exceptions
- Register list views and update
- Multicore development support
- Custom UI
- AndeStar™ V/CPU support
- Extensive demo projects
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- Corvette P1 (Ambarella-Compatible board) support

**Compilation Tools**

- Compiler
- Assembler
- Linker

**Debug/Analysis**

- Debugger
- Profiler
- Code Coverage
- Code Size

**AndesSight™ IDE**

- Managed Build System
- Debugger Interface
- Profiler Interface
- Target Management

**Compilation Tools**

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**AndesSight™ IDE**

- Managed Build System
- Debugger Interface
- Profiler Interface
- Target Management

**Toolchains**

- Compiler for ELF and Linux targets
- Andes efficient ROM path solution
- Highly optimized DSP library functions
- Highly optimized 3D functions

**Simulator**

- CPU simulation
- Test cycle accurate
- Mode of AndesChip™ SoC platform

**ICE**

- Nice, debugger (4-wire/2-wire)
  with OpenOCD support

**Supported Host Platforms**

- Windows 7 / Windows 10
- Ubuntu Linux 16.04 / ComOS 6.6
- Red Hat Linux 6.6

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