Plus1 Architecture Introduction

For New, Innovated, and Niche Markets

Smart Computing Program
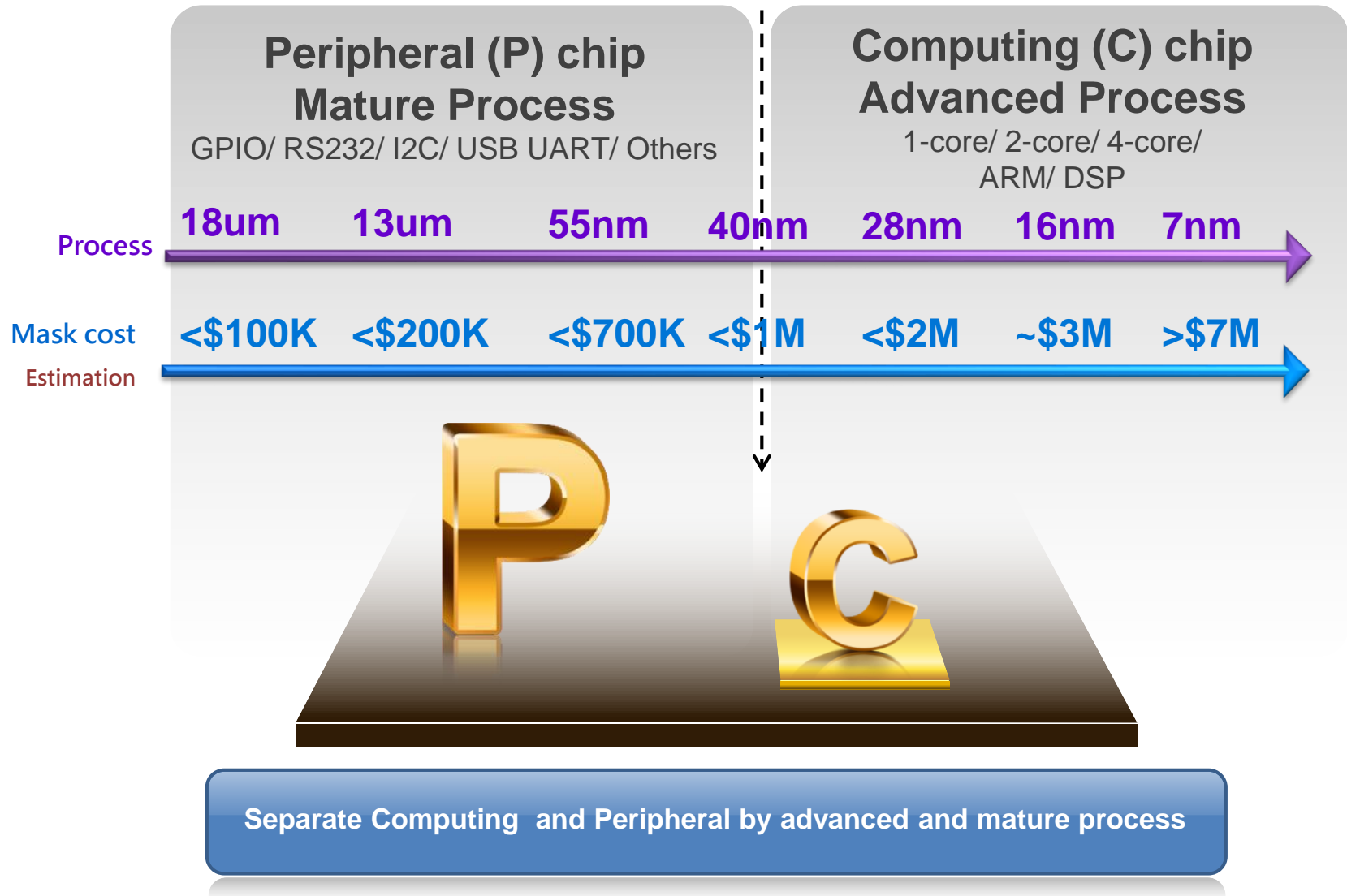
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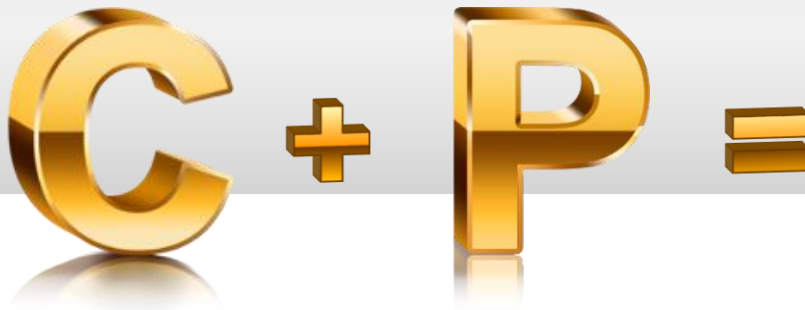
Make difference

Introduction

- Expensive NRE for advanced processes:
  - Main stream market: Mobile phone, GPU, FPGA, …
  - NRE includes: IP license, Pilot Run, Mask, RD cost, CAD tools...
- New, innovated or niche markets:
  - Not market feasible for advanced processes
- Advanced process has good C/P for <u>logic and memory</u> but not for <u>peripheral or analog designs</u>.
  - Sunplus Plus1 architecture provides a solution to combine mature and advanced process for new, innovated and niche markets.
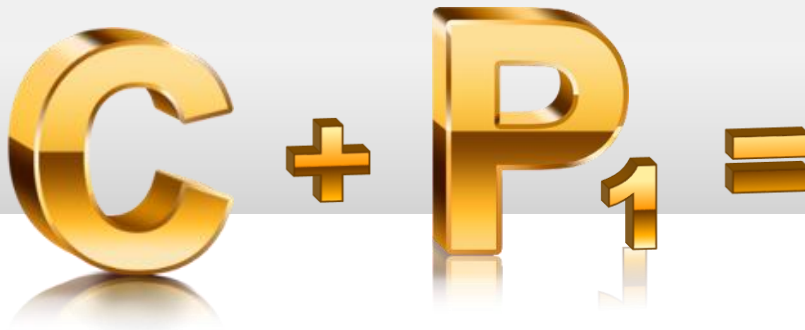
Sunplus Plus1 Architecture

	Peripheral (P) chip Mature Process GPIO/ RS232/ I2C/ USB UART/ Others				Computing (C) chip Advanced Process 1-core/ 2-core/ 4-core/ ARM/ DSP		
Process	18um	13um	55nm	40nm	28nm	16nm	7nm
Mask cost **Estimation**	<$100K	<$200K	<$700K	<$1M	<$2M	~$3M	>$7M

Separate Computing and Peripheral by advanced and mature process

C+P to form Plus1 Solution

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C+P thru CIO and PIO

CIO: "Plug" on C chip

PIO: "Socket" on P chip

Connect C and P thru wire bond

All interface singles thru P chip
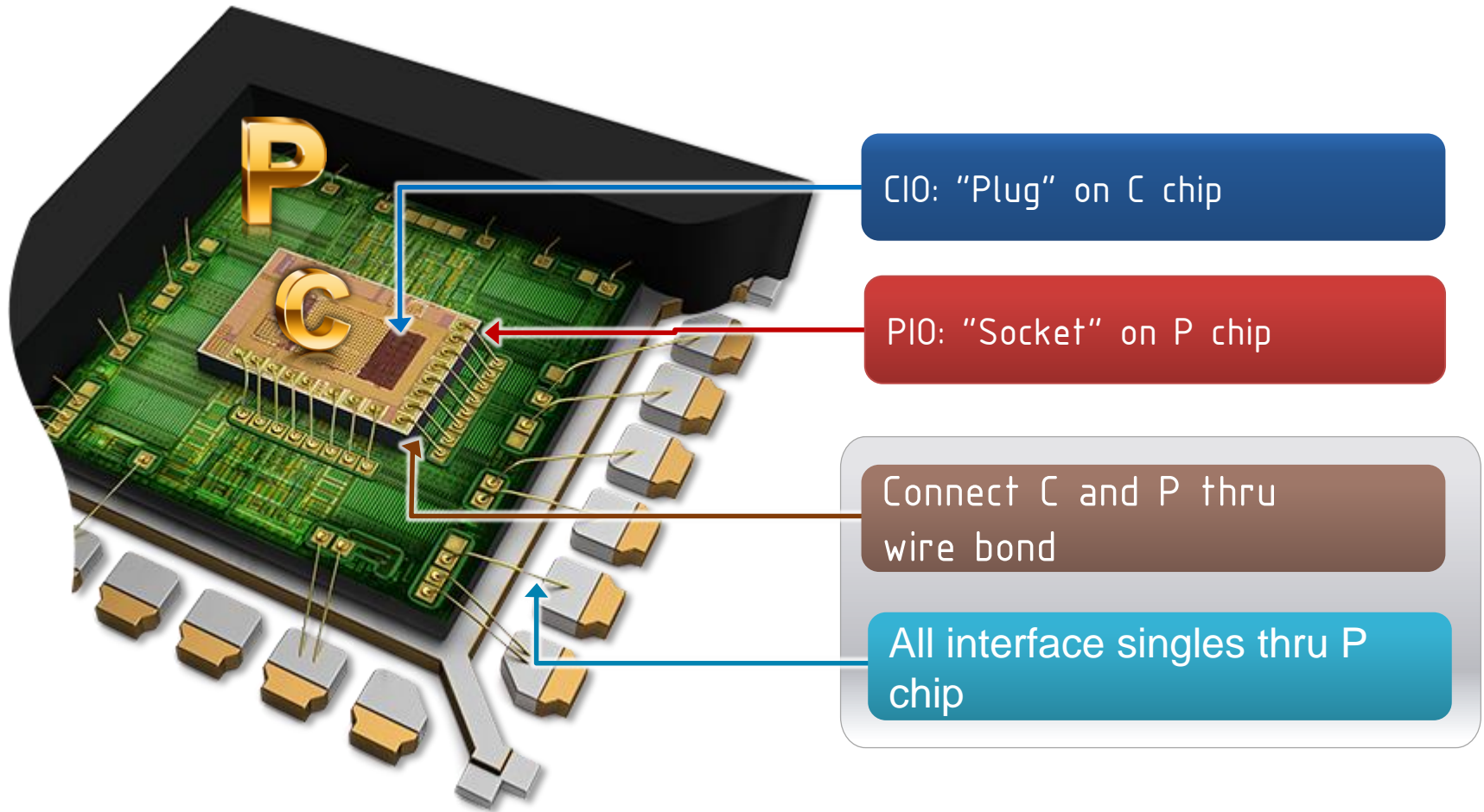
Ideas

New market and new application

<E.g., Drone>

Current	New C+P Model	
P corp.	C corp. C-chip	P corp. P-chip
P	**C** +	**P**
Simple Function	**Advanced Function**	
Up/DN/LF/RT/Stop	**Up/DN/LF/RT/Stop** **Intelligent decision and stability**	

Con:
  a. Few computing power
  b. Simple functions

Pro:
  a. Good computing power
  b. Ready for Complex algorithm
  c. New application style

Plus1 Successful stories: Sunplus + Tibbo

SP7021: The First Plus1 SoC with

Make difference

First C-chip Architecture

Retail Computing Chip

Cortex A7 1GHz L1 32K I$/32K D$	Cortex A7 1GHz L1 32K I$/32K D$	512KB Working SRAM (0.5GHz)
Cortex A7 1GHz L1 32K I$/32K D$	Cortex A7 1GHz L1 32K I$/32K D$	DMA
L2 512KB Cache (0.5GHz)		CPIO
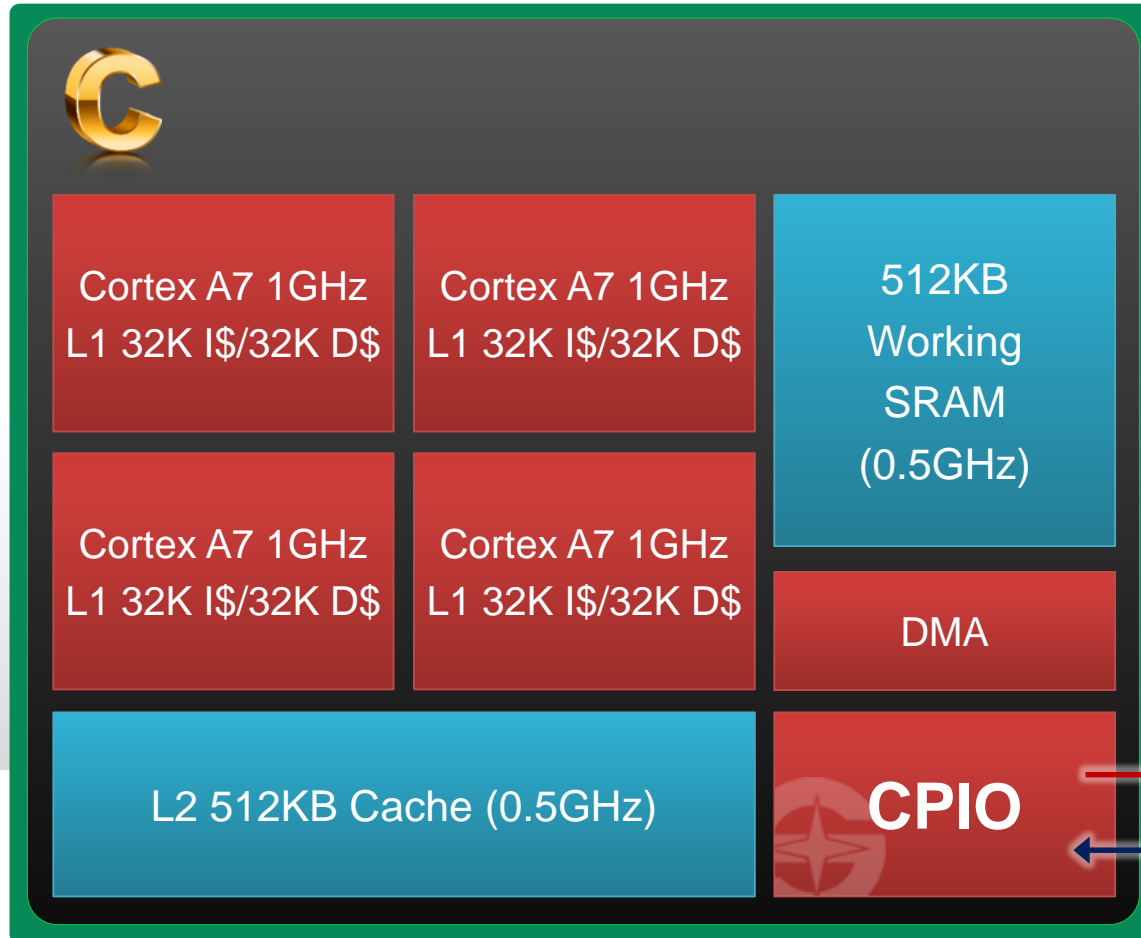
Write → 400MHz * 16 bit * DDR: 1.6GB/s

Read ← 400MHz * 16 bit * DDR: 1.6GB/s

First Plus1 Product: SP7021

New Linux Computing Unit:

Simplicity of a microcontroller

Sophistication of a Linux platform
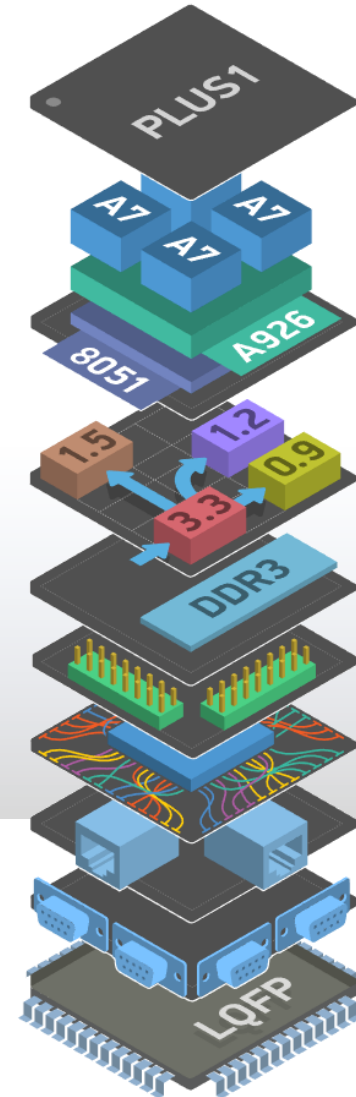
First Plus1 Product: SP7021

## New Linux Computing Unit from Sunplus & Tibbo

- > Raspberry PI 2 Computing Power

- Single 3.3V Power Supply

- Easy for Mass Production

- 64 pins for **ANY** Function combination

- Extendable FPGA interface

- Self-Sustained Linux System

- Wide Range of Applications

SP7021

4-core ARM Cortex-A7 1.0 GHz

Power Mgm. Unit

5 x UART	PWM / Timer
4 SPI / I2C	SDIO / eMMC
9 x GPIO	Ethernet SW
2 x USB	HDMI T x 1.4
ARM926 RTU	8051 MCU

DDR3 4Gb
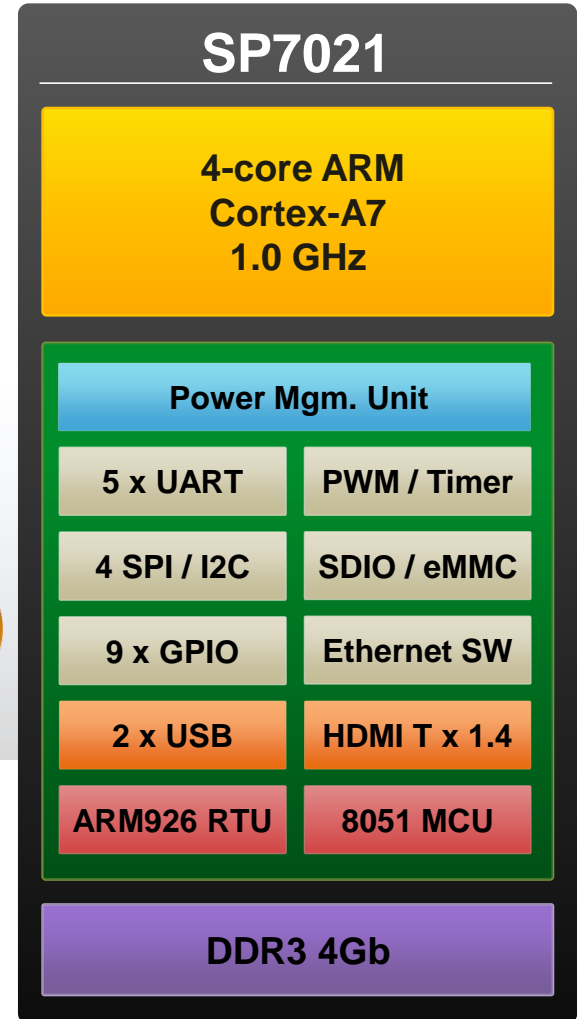
Tibbo Project System with SP7021

Lego approach with Pin Mapping Matrix

■ Pin Mapping Matrix Driver co-work with Tibbo engineers

■ Built-in DDR3 & DC/DC brings the smallest PCB size
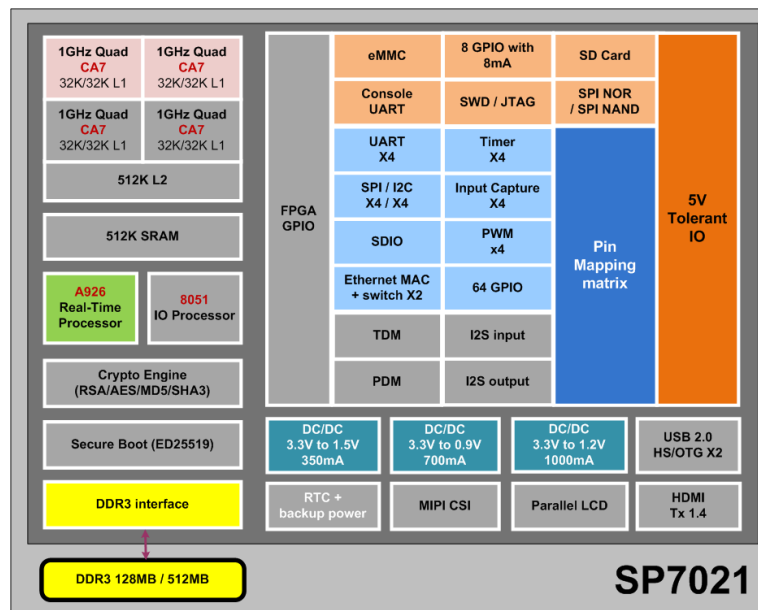
SUNPLUS SP7021 Inside

IoT Module

General Purpose SDK

Plug and Play type of features

Results: Easy for Mass Production

- **Pin Mapping Matrix & LQFP176**

- **4Gb DDR Integrated & Single 3.3V Power Supply**

TI based design

Plus1 based design

TI AM335x-based design. 6-layer board. Wire hell.

Plus1-based design. 4-layer board. Simple as a microcontroller circuit.
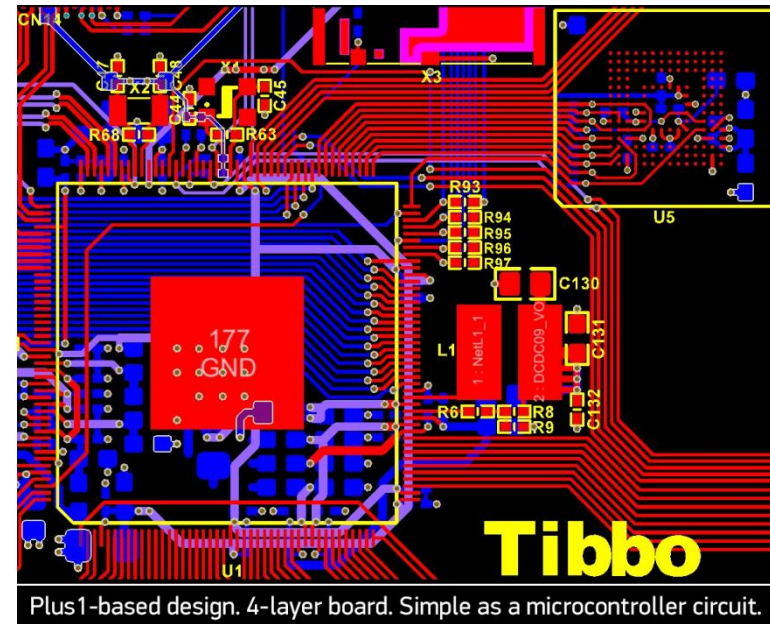
Easy for MP

Value Proposition

Positioning: Overcome the Chasm for Innovation

Chasm for Technology Adoption

Innovators | Early Adopters | Early Majority

"The Chasm"

Higher Volume

IP License

SoC

C$_{IP}$ + P1

Low NRE — High NRE

ASIC

C P1

*P1=FPGA

Plus1: C+P

Lower Cost FPGA

Less Volume
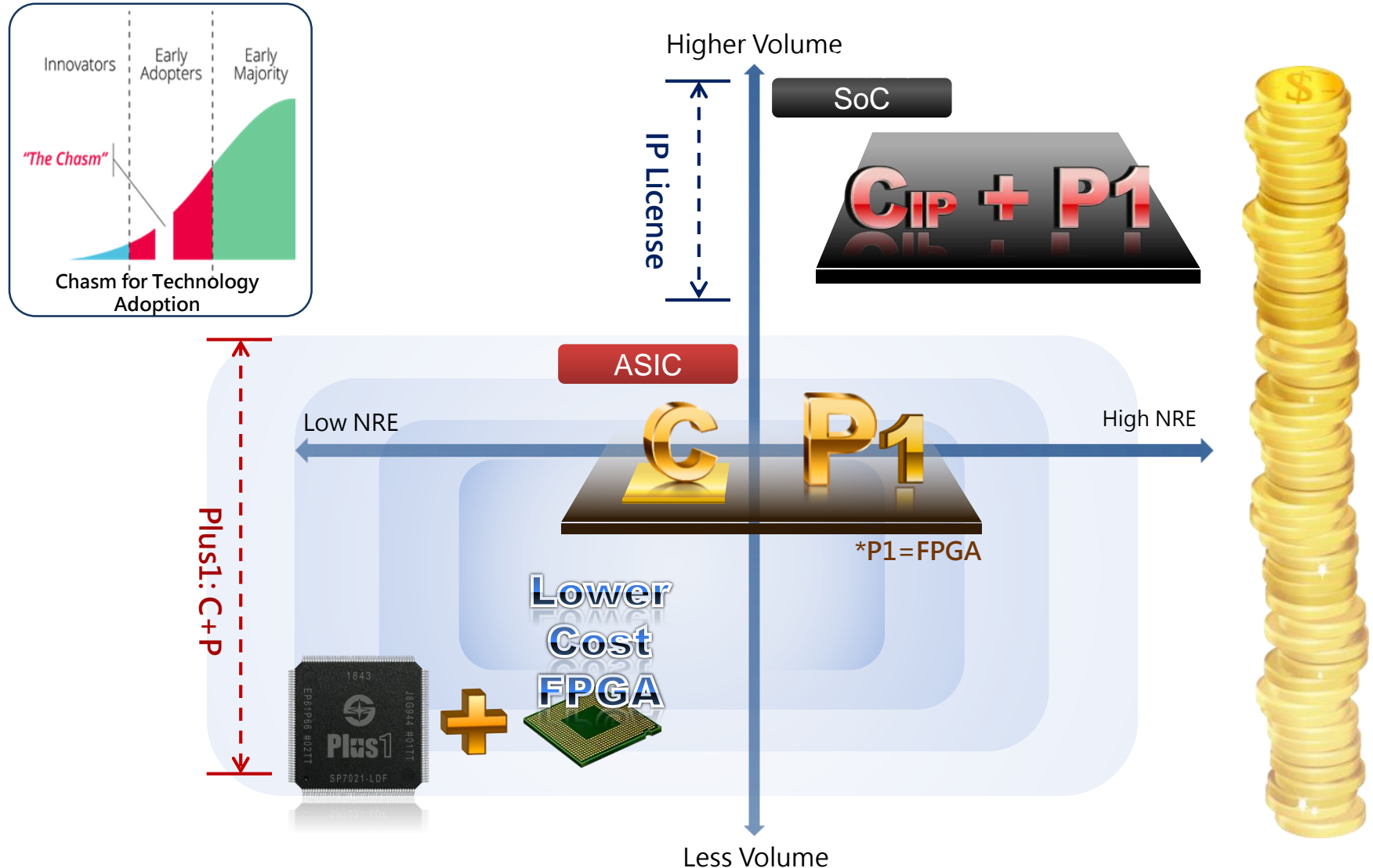
Flourish IC Design ECO System

Low Entry Barrier / Easy Startup / School Innovative

C-Chip/PIO (C Company)

CIO

Design/System Houses

Startup

PIO

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Design/ASIC Service

Brite

VeriSilicon

GUC

Faraday

PGC
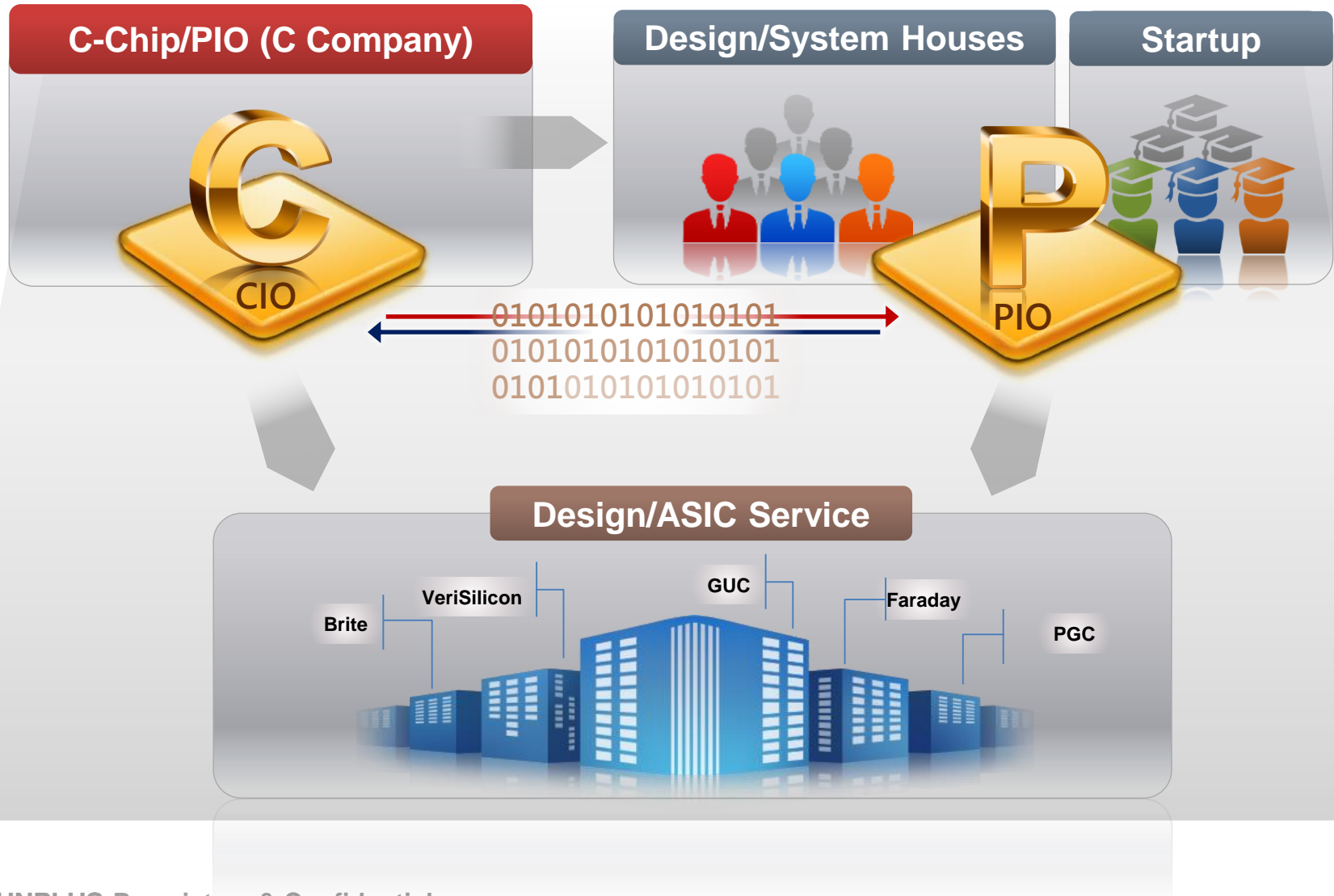
Open Platform:

SP7021 Online Documents

人臉辨識 Demo：SP7021+NN加速棒

■ 1週內自行完成人臉辨識 Demo：SP7021+NN加速棒

━ 參考影片：https://www.youtube.com/watch?v=M0lsRZ5Exaw&feature=youtu.be

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