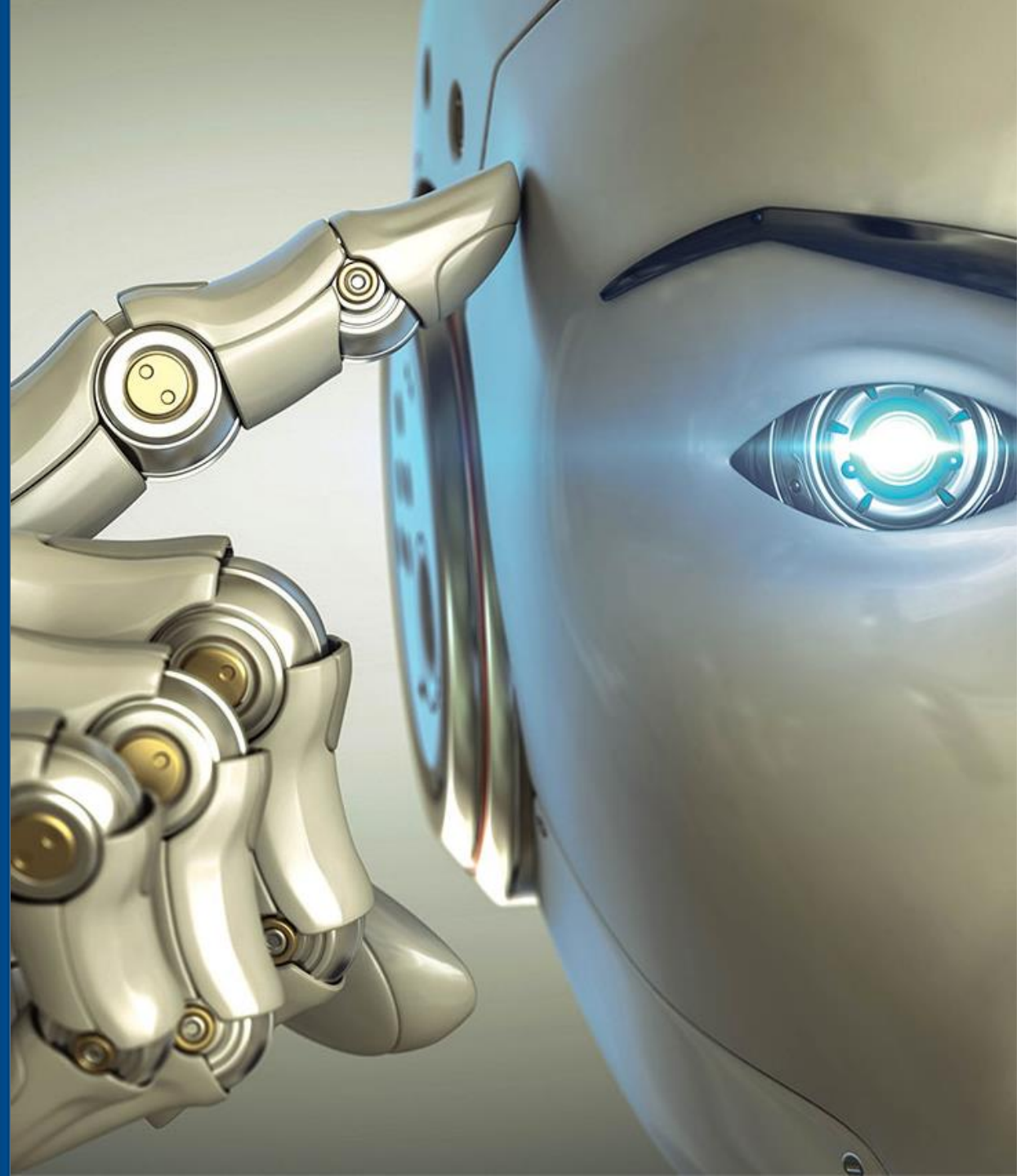
Lateral power to Vertical power
橫向功率到垂直功率傳輸

FAE

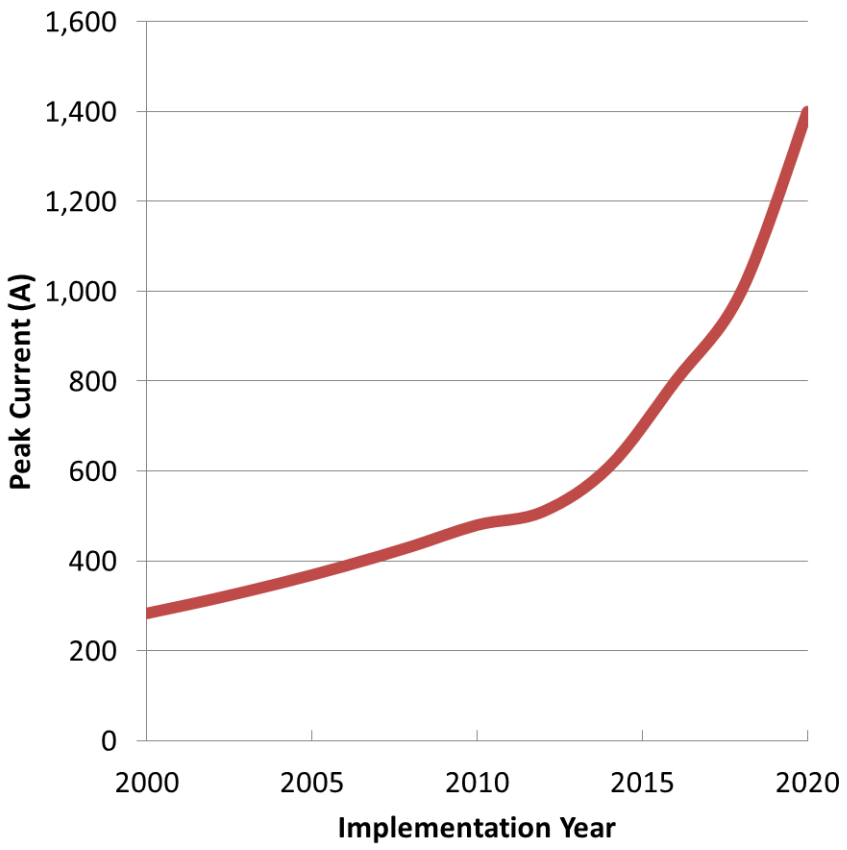
楊有承 Nathan Yang



Enabling the Highest Performance AI Accelerators with Vertical Power Delivery

Challenge in Powering AI Processors

- Increasing power
  - Decreases power efficiency
    - increasing distribution losses
  - Constrains system design
    - power consumes more board area
  - Sacrifices the quality of power delivered
    - added parasitics
  - Increases thermal demands
    - how to keep cool?
  - Can limit XPU operating performance if power demands are not met



Progression of Customer CPU/GPU Peak Current Requirements

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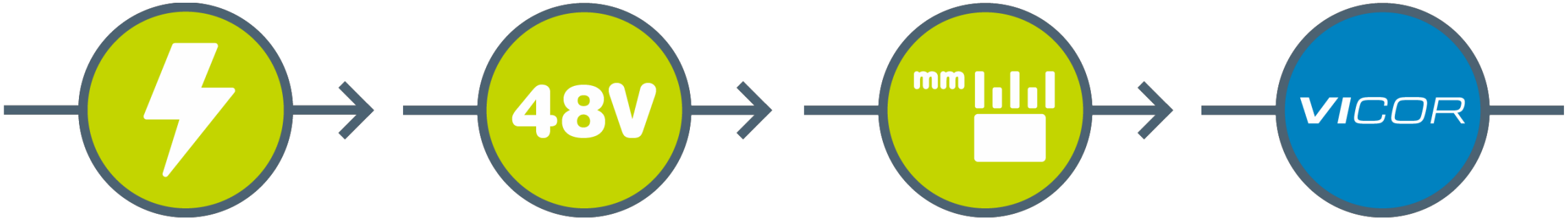
Power Distribution Networks (PDN)



System performance demands drive rapidly increasing load power

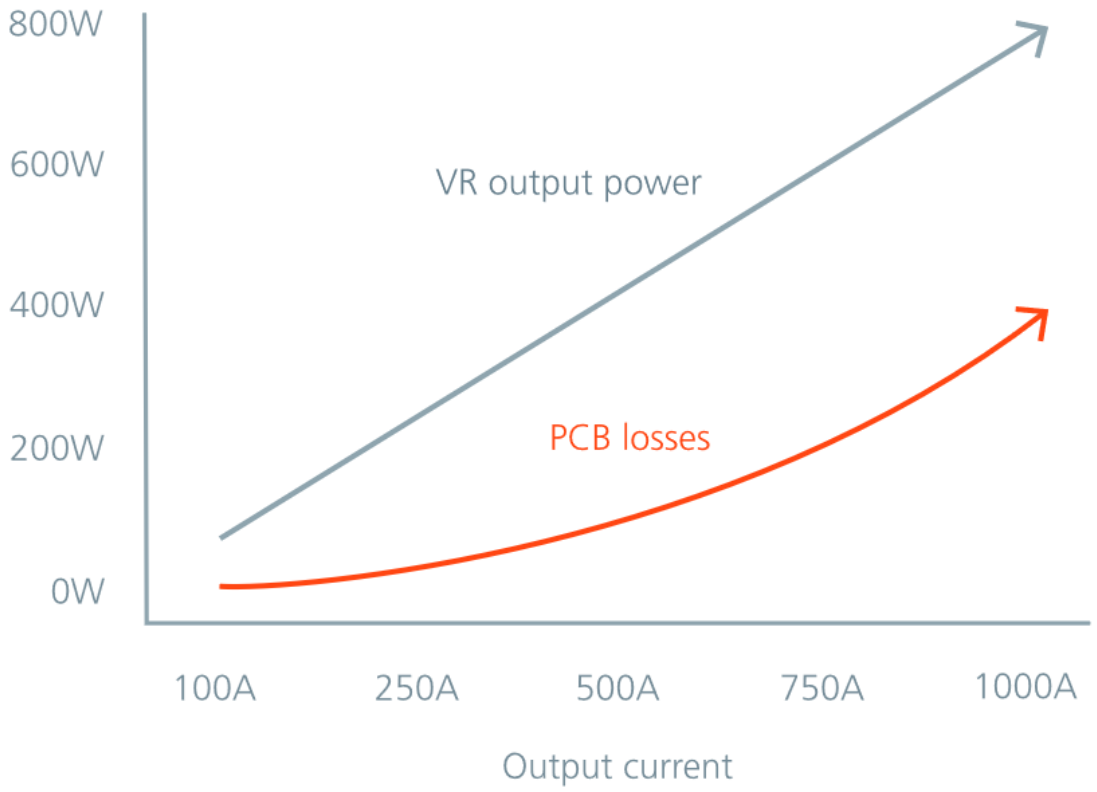
Moving PDN to higher voltages eases the delivery and distribution of higher power

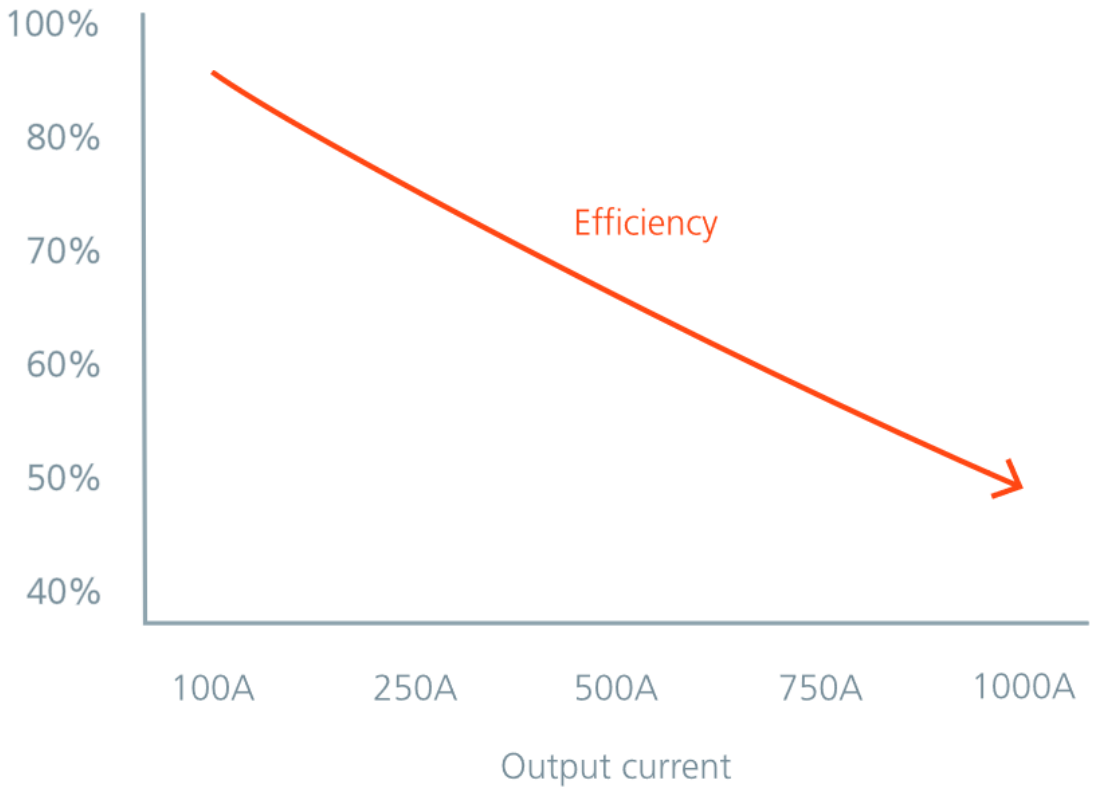
Power = Voltage x Current

High-density needed at the point of load to increase performance and efficiency

The power module company with, ***by far***, the highest performance and density

Power distribution loss from the VR to the processor





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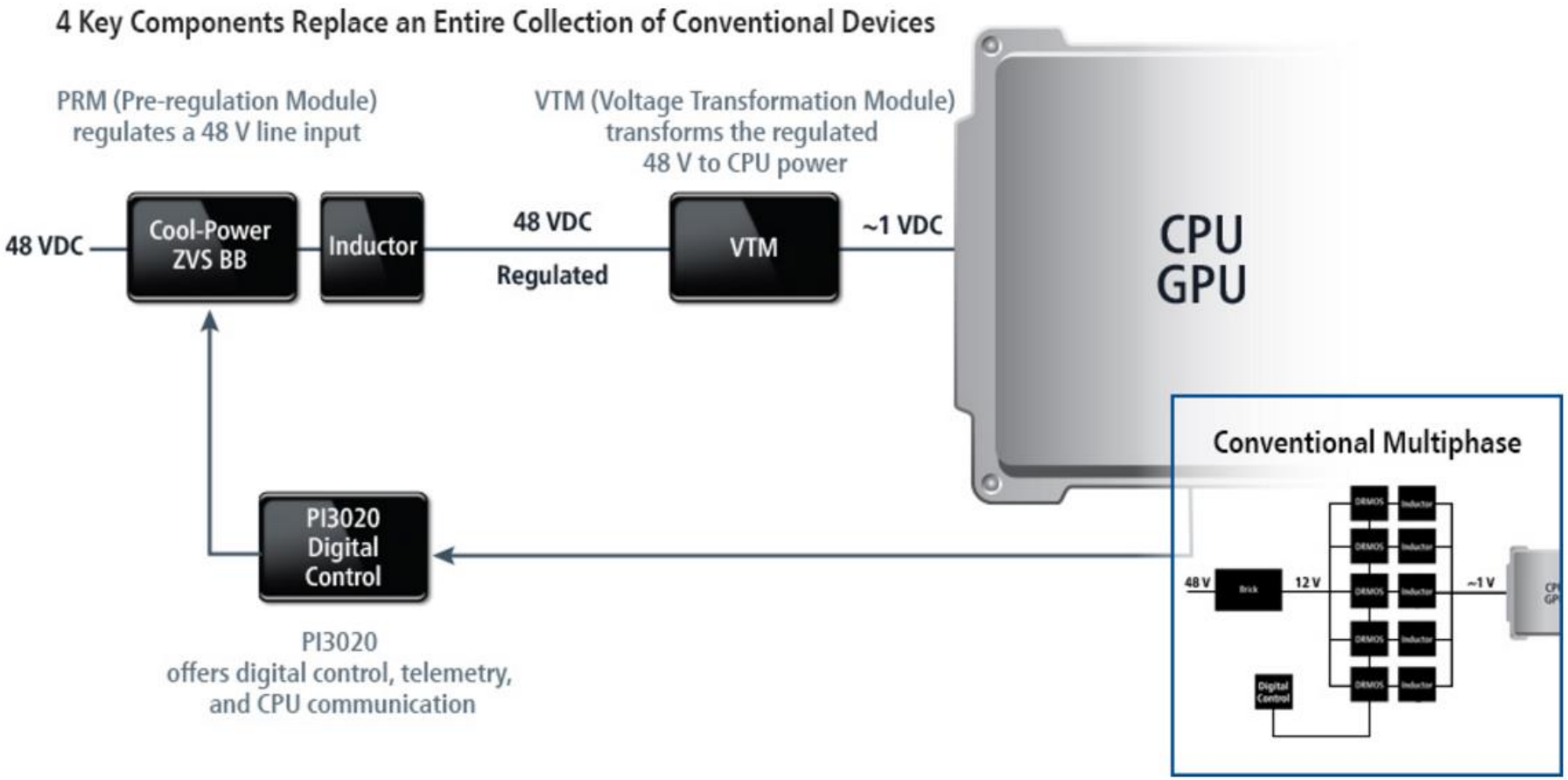
48 V Direct to CPU : Single Stage Conversion



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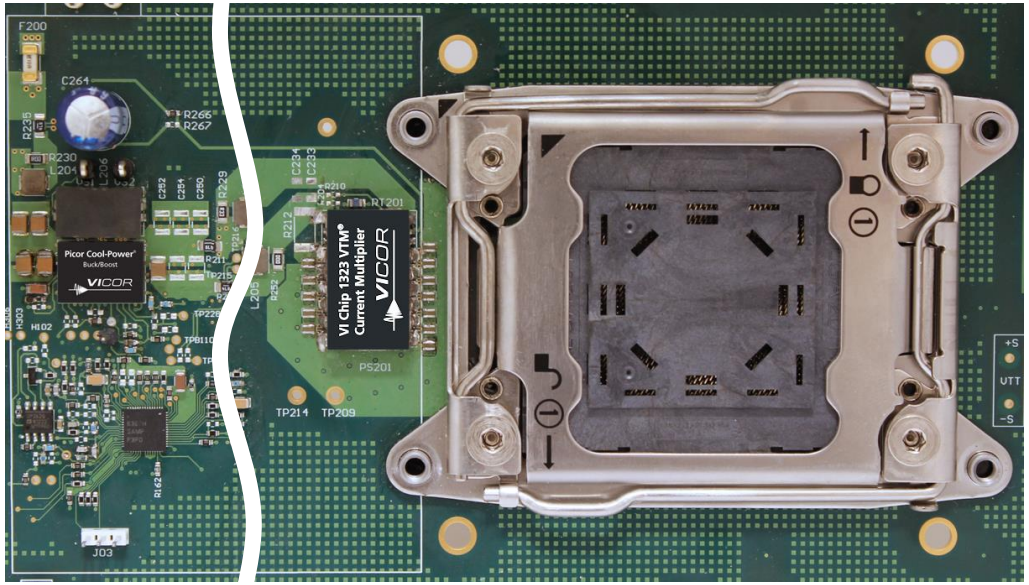
PDN of VR13 Board



PRM and controller placed on board edge

Only VTM itself placed by CPU

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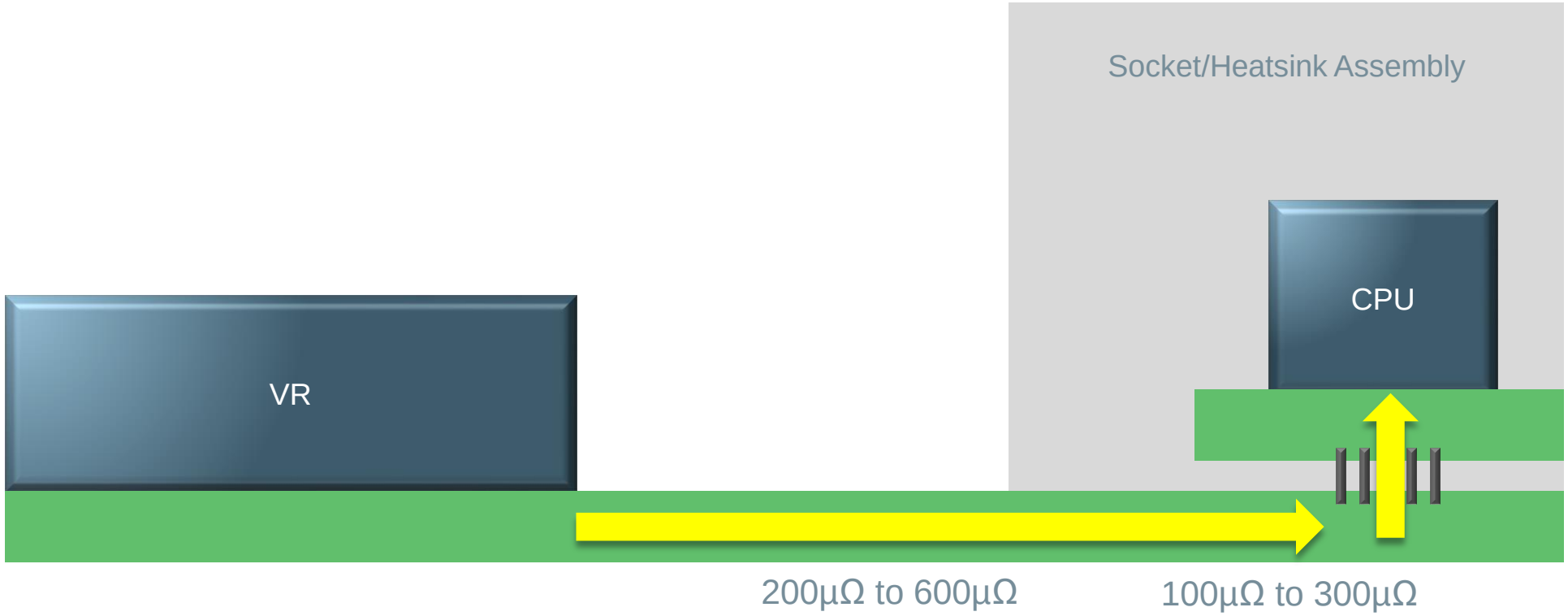
The Last Mile (Last Inch)



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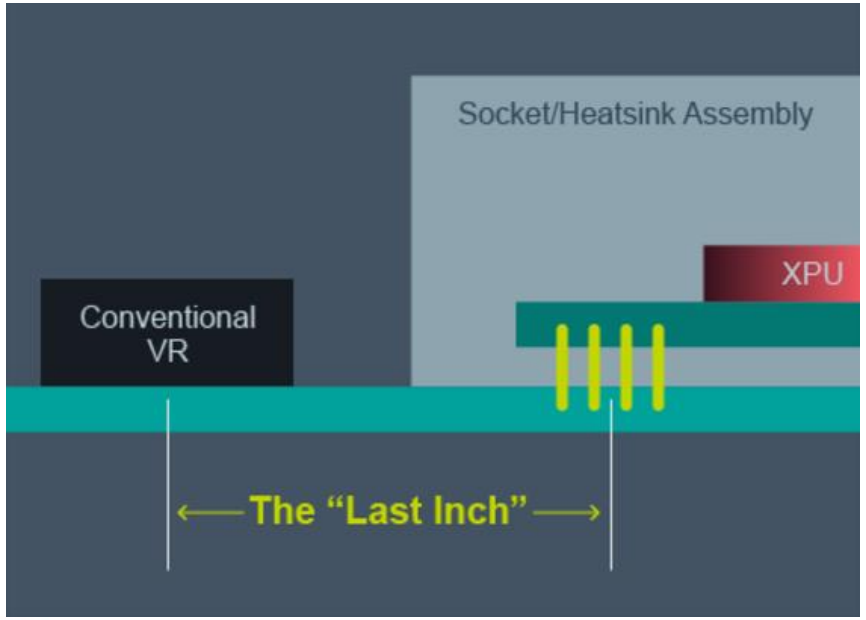
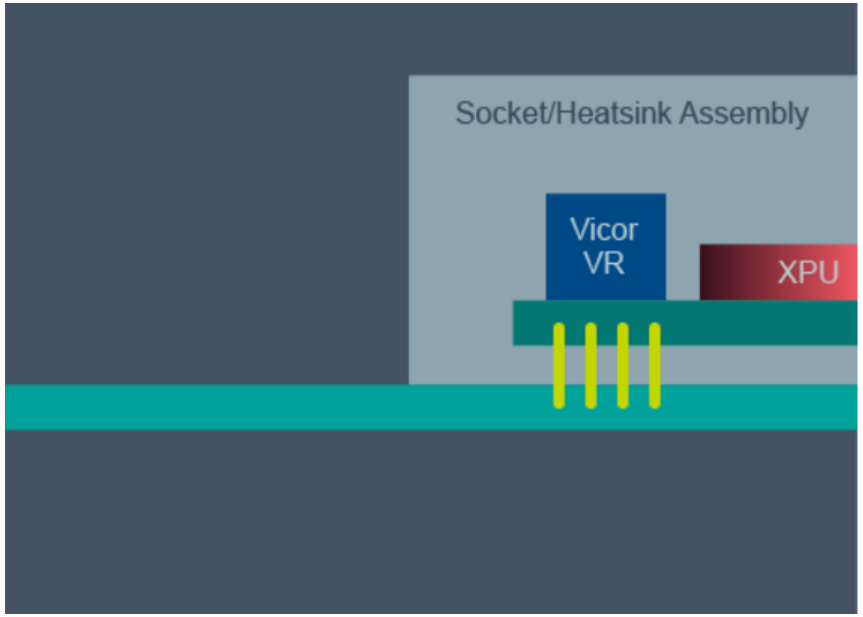
Power on Package – Eliminates the Last Inch

- Power-on-Package practically eliminates the power delivery network
- Moves high current delivery from the VR off the motherboard and places it adjacent to the XPU
- Power-on-Package solution enables higher current delivery for maximum XPU performance





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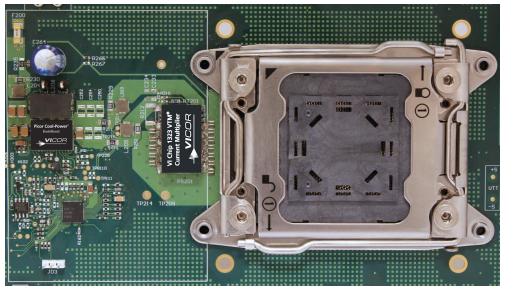
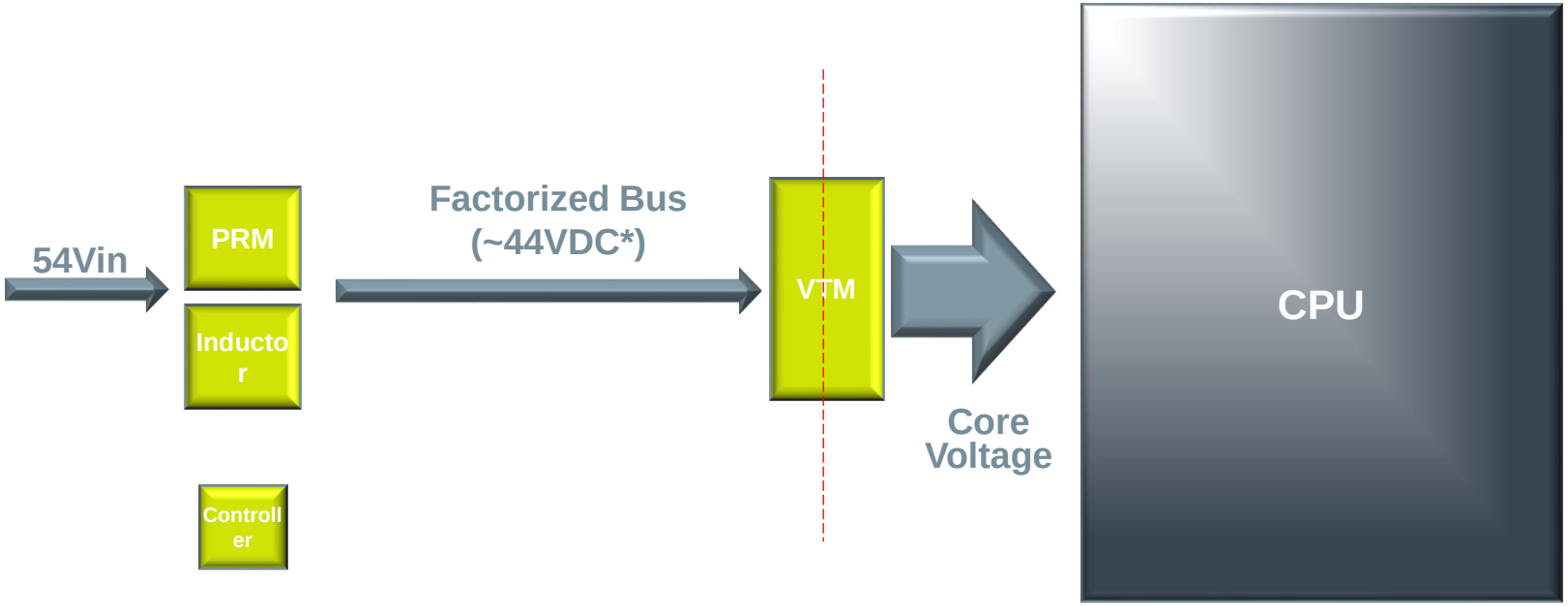
48V Direct to CPU

How to Eliminates the Last Inch??

PRM/VTM Re-partitioned to MCD/MCM





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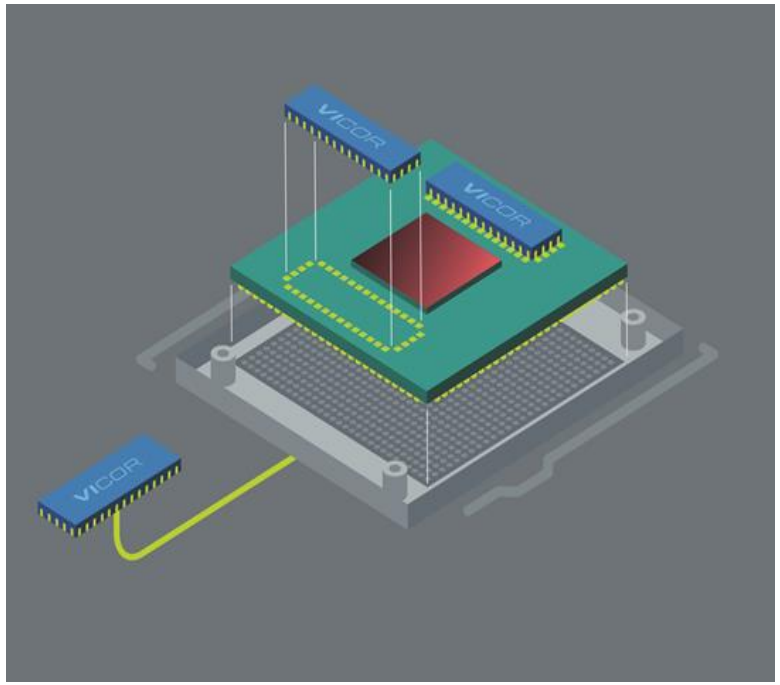
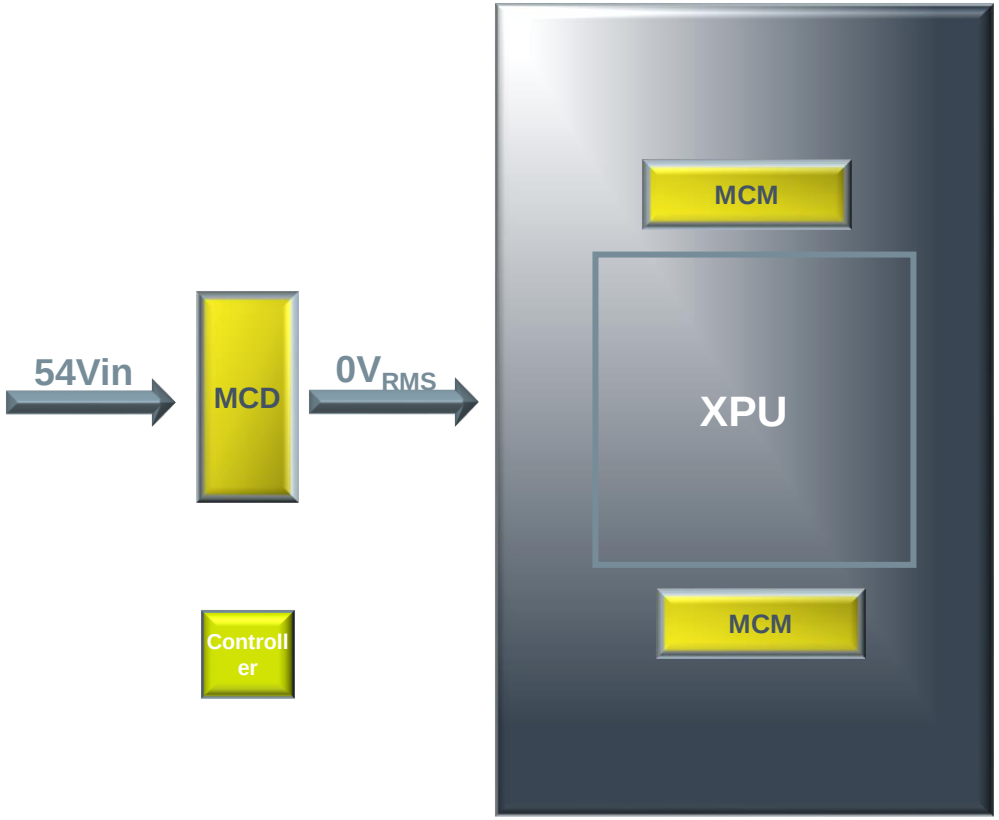
48V Direct to CPU

MCD/MCM Power on Package





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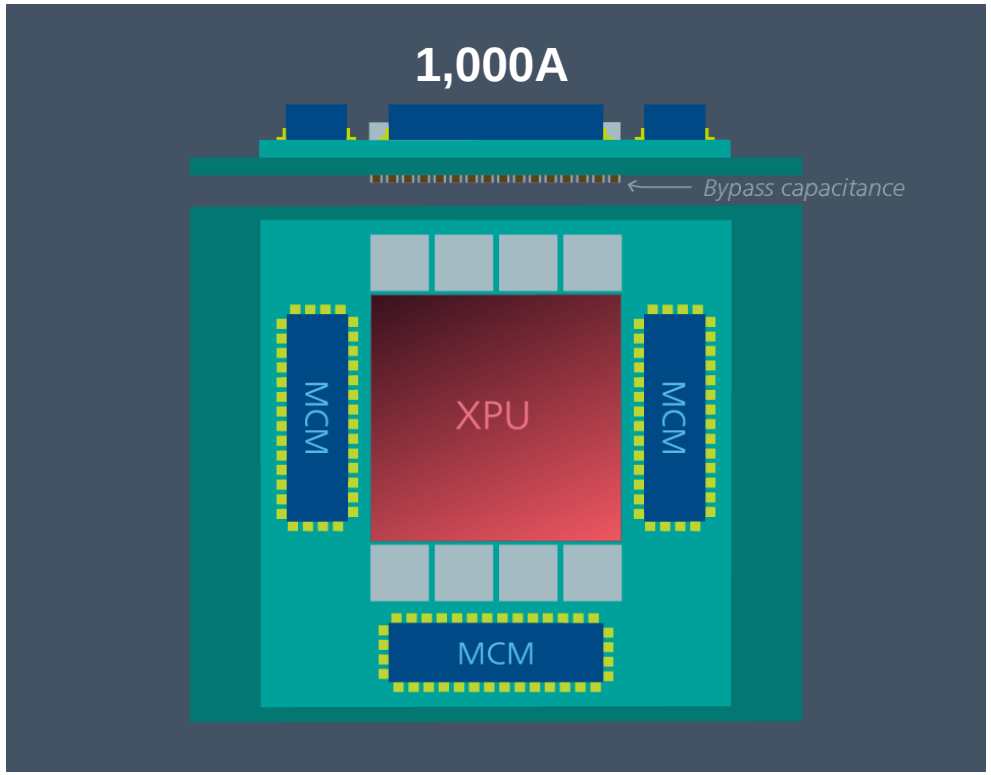
Lateral Power Delivery : Power-on-Package

- MCMs mounted on sides of XPU
- Reduces PDN losses
- Reduces server board layer count
- Improves transient performance
- Extends peak current capability to >1,000A



Lateral Power Delivery (LPD)

Typical PDN resistance: 70µΩ

PDN loss at 1,000A: 70 Watt

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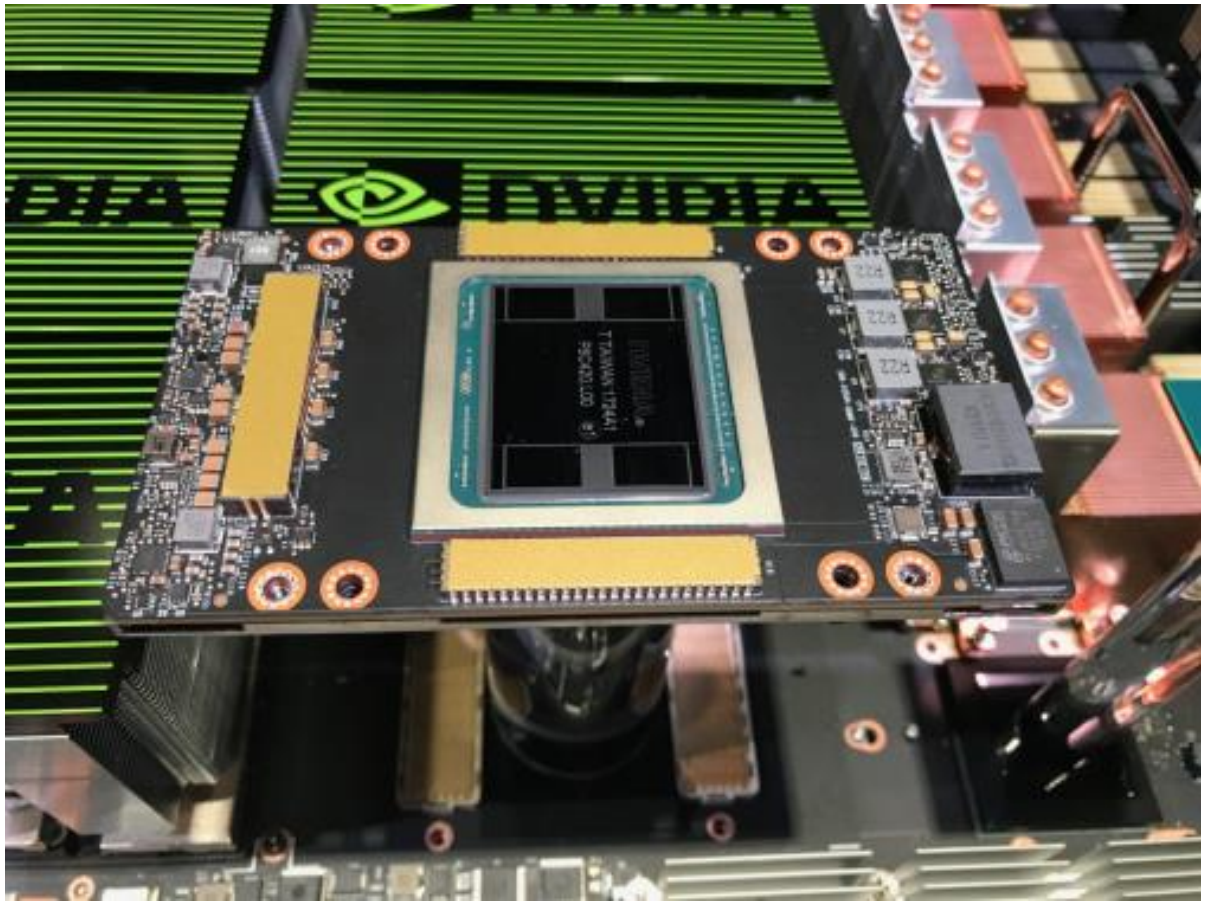
Comparison of 12V Multiphase vs. Factorized Power

Older Nvidia SXM2 Card
Using
Conventional 12V Multiphase



Latest, higher power, Nvidia SXM3 Card
Using
48V Vicor Power-on-Package

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Gyoukou Server

System Enabled by Power on Package

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Does Lateral Power Delivery Good Enough?

The Last Mile (Last Inch)

40μΩ to 70μΩ

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Enabling the Highest Performance AI accelerators with…
Vertical Power Delivery

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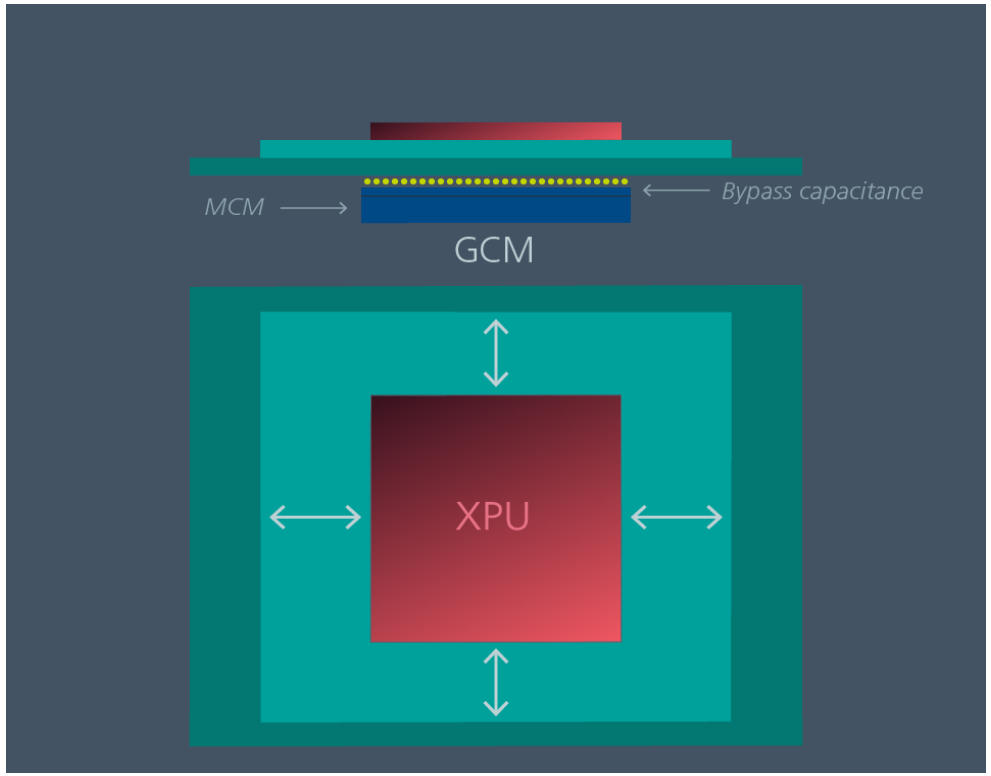
Vertical Power Delivery

- MCM mounted on bottom of XPU
- Reclaims valuable space around the XPU
- Minimizes PDN loss
- Integrates PoL capacitance
- Maximizes system efficiency
- Maximizes XPU performance

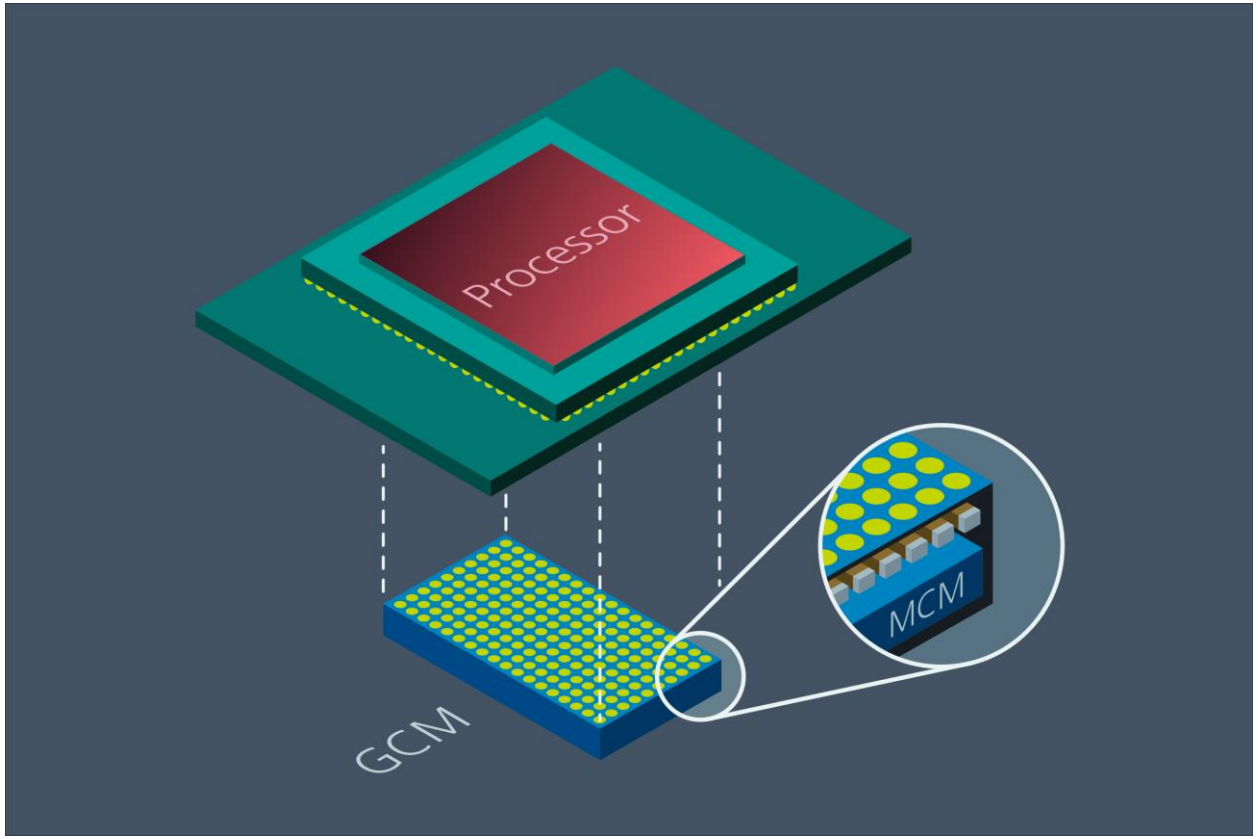


Vertical Power Delivery (VPD)

Typical PDN resistance: 10µΩ

PDN loss at 1,000A: 10 Watt

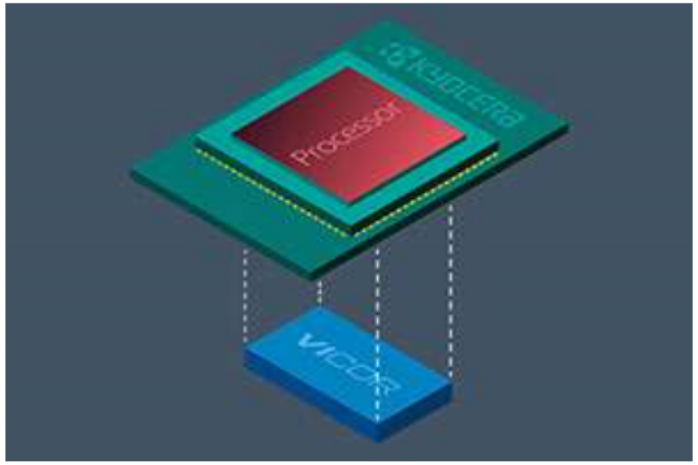
Vertical Power Delivery



For Immediate Release

Semiconductor Industry: KYOCERA and Vicor to Collaborate on Advanced Power-on-Package Solutions

Collaboration will maximize Artificial Intelligence performance and minimize time-to-market for new processor designs

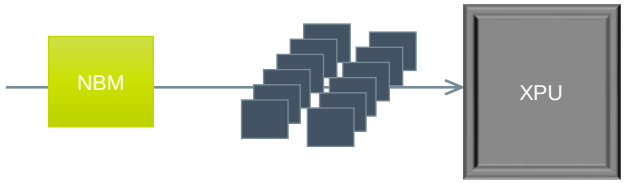


Andover, MA and Kyoto, Japan – April 10, 2019 – Kyocera Corporation (TOKYO:6971) and Vicor Corporation (NASDAQ:VICR) – will collaborate on next-generation Power-on-Package solutions to maximize performance and minimize time-to-market for emerging processor technologies, the companies announced today. As a part of the collaboration between the two technology leaders, Kyocera will provide the integration of power and data delivery to the processor with organic packages, module substrates and motherboard designs. Vicor will provide Power-on-Package current multipliers enabling high density, high current delivery to processors. This collaboration will address the rapid growth of higher performing processors, which has created proportionate growth and complexity in high-speed I/Os and high current consumption demands.

Vicor's Power-on-Package technology enables current multiplication within the processor package, allowing for higher efficiency, density, and bandwidth. Providing current multiplication within the package can reduce interconnect losses by up to 90 percent, while allowing processor package pins, typically required for high current delivery, to be reclaimed for expanded I/O functionality. Vicor's Power-on-Package solutions were featured at the NVIDIA GPU Technology Conference 2018 and China ODCC 2018 Summit. Vicor's advanced Power-on-Package technology enables Vertical Power Delivery (VPD) from the bottom side of the processor. VPD virtually eliminates Power Delivery Network (PDN) losses while maximizing I/O capability and design flexibility.

Kyocera's proprietary solutions to optimize processor performance and reliability are based on decades of experience in package, module and motherboard manufacturing for customers worldwide. Kyocera has cultivated design expertise by applying Vicor's Power-on-Package devices in multiple applications. By utilizing its design technology, simulation tools and manufacturing experience, Kyocera provides optimal designs for complex I/O routing, high speed memory routing, and high-current power delivery. Through collaboration, Kyocera and Vicor will bring new solutions for AI and high-performance processor applications to market.

Summary of 48V VR PoL Options

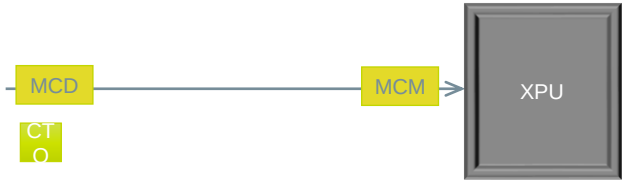


NBA - NBM to Multiphase

- Re-use existing Multiphase design
- Commonality between 12V and 48V server solutions

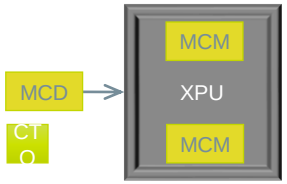
48V Direct to CPU – PRM/VTM On Motherboard solution

- Higher efficiency & density 48V solution
- Lower noise and faster transient response
- PRM can be remote from prime XPU real estate



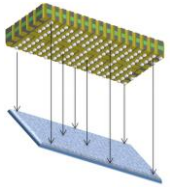
48V Direct to CPU – MCD/MCM On Motherboard solution

- Low profile current multiplier (MCM) placed closer to XPU
- Lower cost, high current XPU solutions >130A



48V Direct to XPU – MCD/MCM Power on Package

- Eliminates interconnect losses (bypassing traditional PDN)
- High efficiency and current capability up to 1000A



48V Direct to XPU – MCD/MCM Power on Chip

- Modular Current Multiplier on Chip
- Highest efficiency and current density

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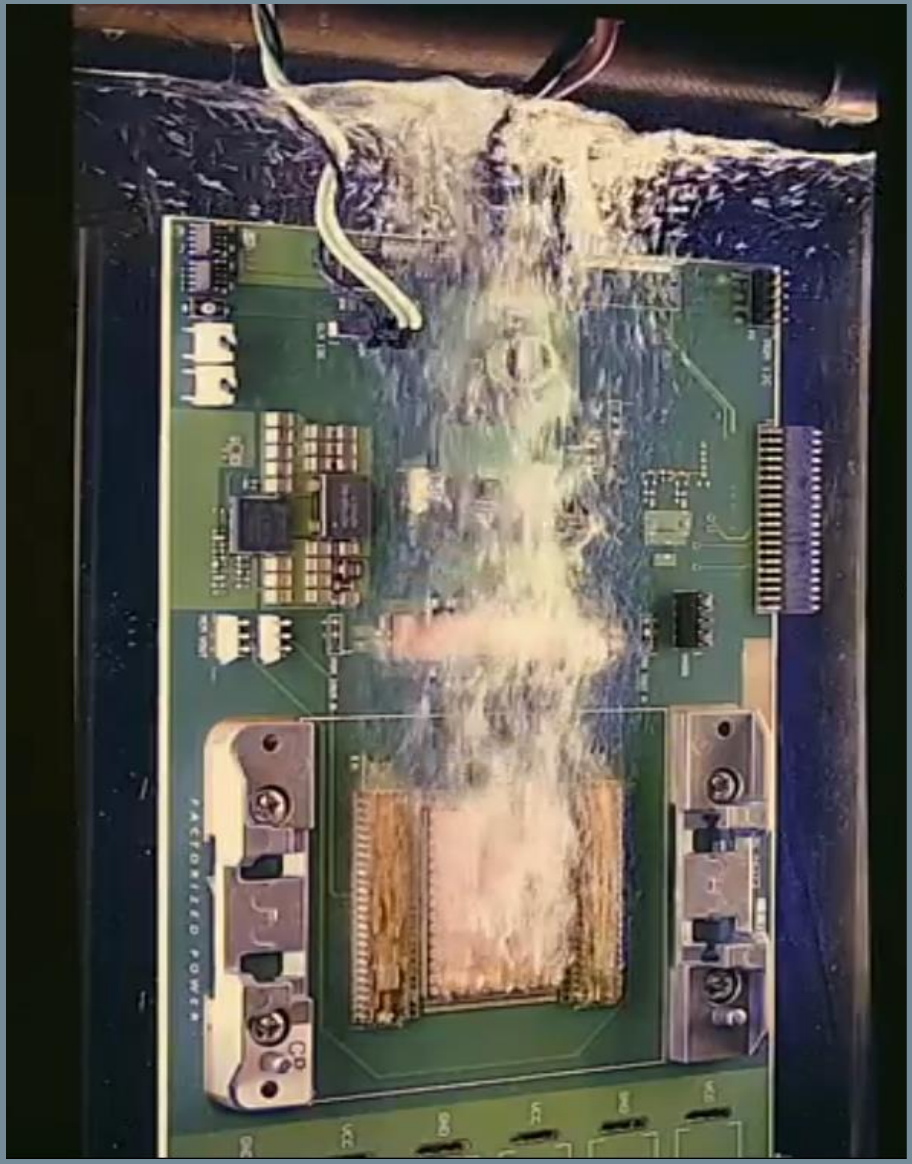

OCP Summit – March 19

Demonstrating Immersion cooling with 3M

VICOR | 3M

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PEZY Gyoukou Server using Vicor front end and Power on Package

Thank you

Questions?